PRELIMINARY

MOSTEK

1Kx8 STATIC RAM

MK4118(P/N)Series

FEATURES

- ☐ Address Activated ™ Interface combines benefits of Edge Activated ™ and fully static.
- ☐ High performance

Part number	Access time	Cycle time
MK4118-1	120 nsec	120 nsec
MK4118-2	150 nsec	150 nsec
MK4118-3	200 nsec	200 nsec
MK4118-4	250 nsec	250 nsec

- ☐ Single +5 volt power supply
- ☐ TTL compatible I/O

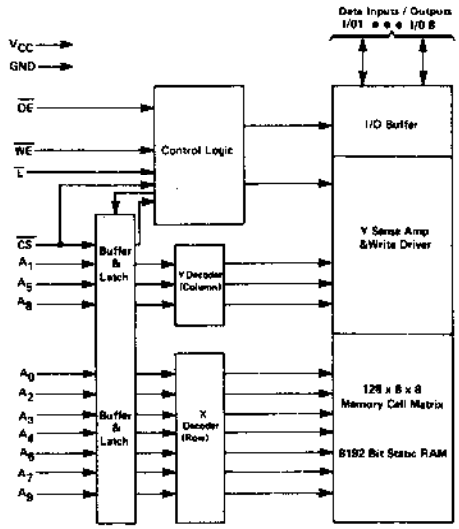
  Fanout: 2 - Standard TTL
  2 - Schottky TTL
  12 - Low power Schottky TTL
- ☐ Low Power - 400mw Active
- ☐ 24-pin ROM/PROM compatible pin configuration
- ☐ $\overline{CS}$, $\overline{OE}$, and $\overline{LATCH}$ functions for flexible system operation
- ☐ Read-Modify-Write Capability

DESCRIPTION

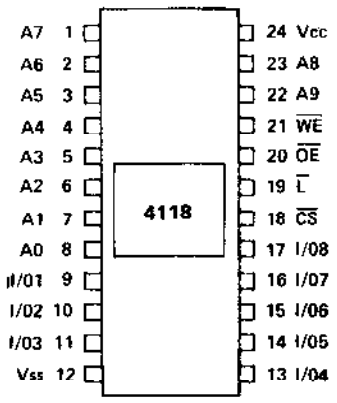
The MK4118 uses MOSTEK's Poly R N-Channel Silicon Gate process and advanced circuit design techniques to package 8192 bits of static RAM on a single chip. MOSTEK's address activated ™ circuit design technique is utilized to achieve high performance, low power, and easy user implementation. The device has a V_{IH} = 2.2, V_{IL} = 0.8V, V_{OH} = 2.4, V_{OL} = 0.4V making it totally compatible with all TTL family devices.

The MK4118 is designed for all wide word memory applications. The MK4118 provides the user with a high-density, cost-effective 1Kx8 bit Random Access Memory. Fast Output Enable ($\overline{OE}$) and Chip Select ($\overline{CS}$) controls are provided for easy interface in microprocessor or other bus-oriented systems. The MK4118 features a flexible Latch ($\overline{L}$) function to permit latching of the address and $\overline{CS}$ status at the user's option. Common data and address bus operation may be performed at the system level by utilizing the $\overline{L}$ and $\overline{OE}$ functions for the MK4118. The latch function may be bypassed by merely tying the latch pin to V_{CC}, providing fast ripple-through operation.

BLOCK DIAGRAM



PIN OUT



PIN NAMES

A0 - A9	Address Inputs
$\overline{CS}$	Chip Select
Vss	Ground
Vcc	Power (+5V)
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
$\overline{L}$	Latch
I/O_1 - I/O_8	Data In/ Data Out Port

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{SS} ..... −0.5V to +7.0V
Operating Temperature T_A (Ambient) ..... 0° C to + 70° C
Storage Temperature (Ambient) (Ceramic) ..... −65° C to +150° C
Storage Temperature (Ambient) (Plastic) ..... −55° C to +125° C
Power Dissipation ..... 1 Watt
Short Circuit Output Current 20mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0° C ≤ T_A ≤ + 70° C)

	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.75	5.0	5.25	Volts	1
V_{SS}	Supply Voltage	0	0	0	Volts	1
V_{IH}	Logic "1" Voltage All Inputs	2.2		7.0	Volts	1
V_{IL}	Logic "0" Voltage All Inputs	−0.3		0.8	Volts	1

DC ELECTRICAL CHARACTERISTICS[1]

(0° C ≤ T_A ≤ + 70° C) (V_{CC} = 5.0 volts ± 5%)

	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	Average V_{CC} Power Supply Current (Active)		80	mA	
I_{CC2}	Average V_{CC} Power Supply Current (Standby)		60	mA	
I_{IL}	Input Leakage Current (Any Input)	−10	10	μA	2
I_{OL}	Output Leakage Current	−10	10	μA	2
V_{OH}	Output Logic "1" Voltage I_{OUT} = −1mA	2.4		Volts	
V_{OL}	Output Logic "0" Voltage I_{OUT} = 4mA		0.4	Volts	

AC ELECTRICAL CHARACTERISTICS[1]

(0° C ≤ T_A ≤ + 70° C) (V_{CC} = + 5.0 volts ± 5%)

	PARAMETER	TYP	MAX	NOTES
C_I	Capacitance on all pins except I/0	4pF		
$C_{I/0}$	Capacitance on I/0 pins	10pF		

NOTES:
1. All voltages referenced to V_{SS}.
2. Measured with 0 ≤ V_I ≤ 5V and outputs deselected

OPERATION

READ MODE

The MK4118 is in the READ MODE whenever the Write Enable control input ($\overline{WE}$) is in the high state. The state of the 8 data I/O signals is controlled by the Chip Select ($\overline{CS}$) and Output Enable ($\overline{OE}$) control signals. The READ MODE memory cycle may be either ASYNCHRONOUS (ripple-through) or SYNCHRONOUS, depending on user control of the Latch Input Signal ($\overline{L}$).

ASYNCHRONOUS READ CYCLE

In the ASYNCHRONOUS READ CYCLE mode of operation, the MK4118 provides a fast address ripple-through access of data from 8 of 8192 locations in the static storage array. Thus, the unique address specified by the 10 Address Inputs (An) define which 1 of 1024 bytes of data is to be accessed. The ASYNCHRONOUS READ CYCLE is defined by $\overline{WE}$ = $\overline{L}$ = High.

ELECTRICAL CHARACTERISTICS
($0°C \leq T_A \leq 70°C$ and $V_{CC} = 5.0$ volts ± 5%)

SYMBOL	PARAMETER	MK4118-1		MK4118-2		MK4118-3		MK4118-4		UNIT	NOTE
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
t_{RC}	Read Cycle Time	120		150		200		250		ns	
t_{AA}	Address Access Time		120		150		200		250	ns	
t_{CSA}	Chip Select Access Time		60		75		100		125	ns	
t_{CSZ}	Chip Select Data Off Time	0	60	0	75	0	100	0	125	ns	
t_{OEA}	Output Enable Access Time		60		75		100		125	ns	
t_{OEZ}	Output Enable Data Off Time	0	60	0	75	0	100	0	125	ns	
t_{AZ}	Address Data Off Time	10		10		10		10		ns	
t_{ASL}	Address To Latch Setup Time	0		0		0		0		ns	
t_{AHL}	Address From Latch Hold Time	40		50		65		80		ns	
t_{CSL}	$\overline{CS}$ To Latch Setup Time	0		0		0		0		ns	
t_{CHL}	$\overline{CS}$ From Latch Hold Time	40		50		65		80		ns	
t_{LA}	Latch Off Access Time		160		200		260		325	ns	
t_{WC}	Write Cycle Time	120		150		200		250		ns	
t_{ASW}	Address To Write Setup Time	0		0		0		0		ns	
t_{AHW}	Address From Write Hold Time	40		50		65		80		ns	
t_{CSW}	$\overline{CS}$ To Write Setup Time	0		0		0		0		ns	
t_{CHW}	$\overline{CS}$ From Write Hold Time	40		50		65		80		ns	
t_{DSW}	Data To Write Setup Time	20		30		40		50		ns	
t_{DHW}	Data From Write Hold Time	20		30		40		50		ns	
t_{WD}	Write Pulse Duration	50		70		95		120		ns	
t_{LDH}	Latch Duration, High		DC		DC		DC		DC	ns	
t_{LDL}	Latch Duration, Low		DC		DC		DC		DC	ns	
t_{WEZ}	Write Enable Data Off Time	0	60	0	75	0	100	0	125	ns	
t_{LZ}	Latch Data Off Time	10		10		10		10		ns	

ASYNCHRONOUS READ CYCLE (Cont'd)

A transition on any of the 10 address inputs will disable the 8 Data Output Drivers after t_{AZ}. Valid Data will be available to the 8 Data Output Drivers within t_{AA} after all address input signals are stable, and the data will be output under control of the Chip Select ($\overline{CS}$) and Output Enable ($\overline{OE}$) signals.

SYNCHRONOUS READ CYCLE

The SYNCHRONOUS READ CYCLE is also defined by the Write Enable control input ($\overline{WE}$) being in the high state, and it is synchronized by proper control of the Latch ($\overline{L}$) input.

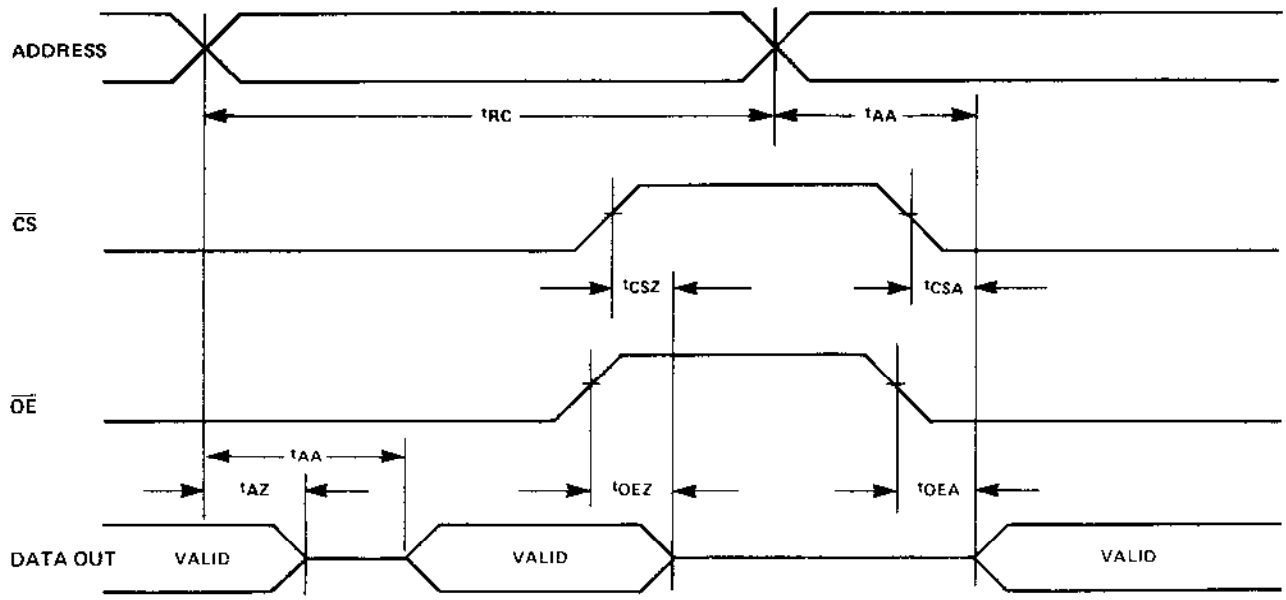
As the Latch control input ($\overline{L}$) is taken low, Address (An) and Chip Select ($\overline{CS}$) inputs that are stable for the specified set-up and hold times are latched internally. Data out corresponding to the latched address will be supplied to the Data Output drivers. The output drivers will be enabled to drive the Output Data Bus under control of the Output Enable ($\overline{OE}$) and latched Chip Select ($\overline{CS}$) inputs.

Taking the latch input high begins another read cycle for the memory locations specified by the address then appearing on the Address Input (An). Returning the latch control to the low state latches the new Address and Chip Select inputs internally for the remainder of the SYNCHRONOUS READ CYCLE.

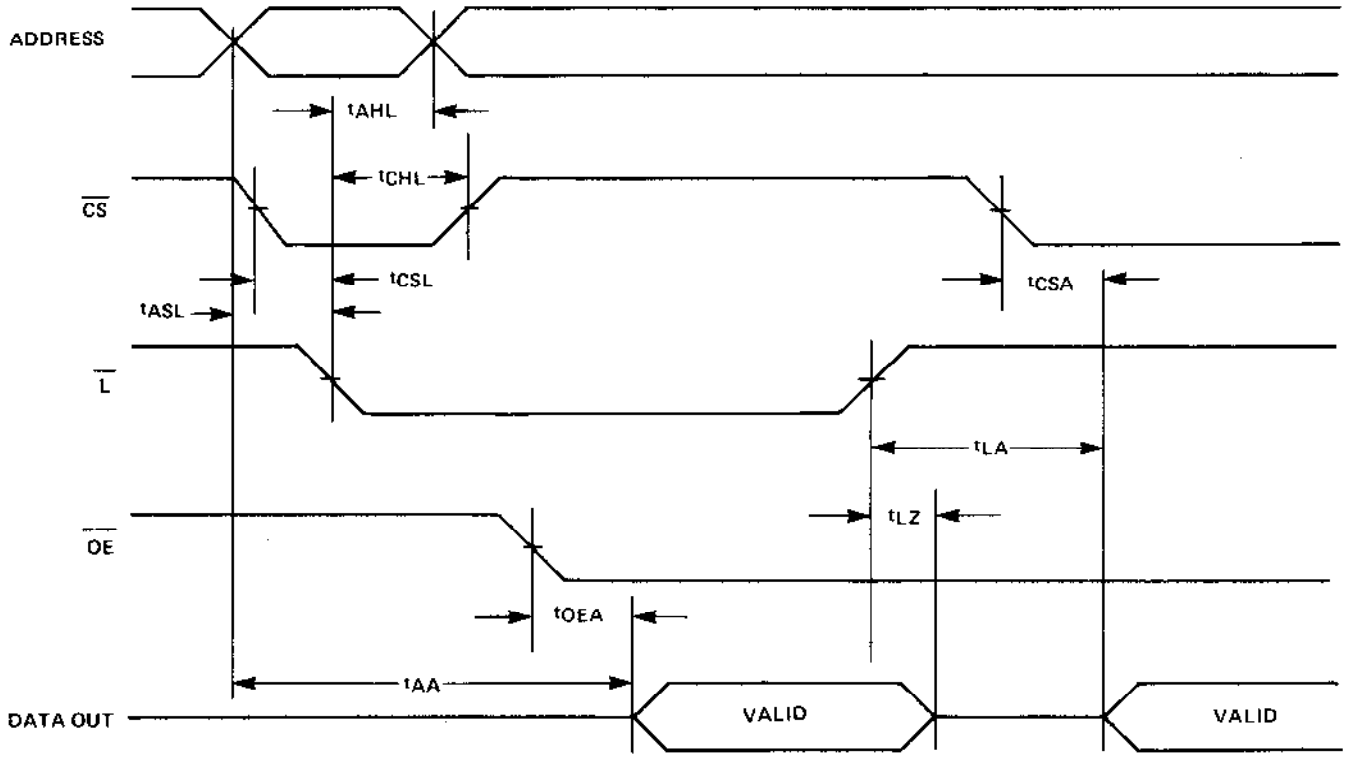
WRITE MODE

The MK4118 is in the WRITE MODE whenever the Write Enable ($\overline{WE}$) and Chip Select ($\overline{CS}$) control inputs are in the low state. The status of the 8 output buffers during a write cycle is expalined below.

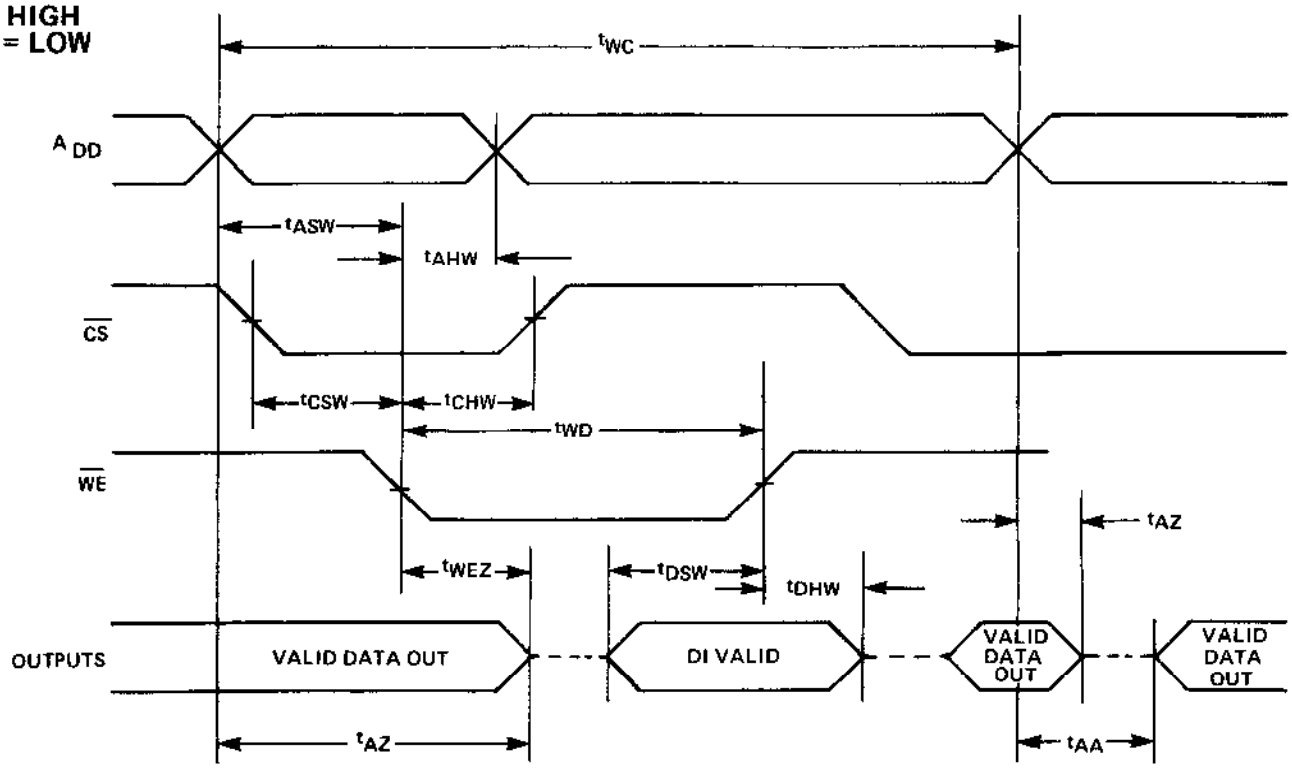
ASYCHRONOUS READ CYCLE
$\overline{WE}$ = $\overline{L}$ = HIGH



SYNCHRONOUS READ CYCLE
$\overline{WE}$ = HIGH



WRITE CYCLE
$\overline{L}$ = HIGH
$\overline{OE}$ = LOW



WRITE MODE (Cont'd)

The WRITE cycle is initiated by the $\overline{WE}$ pulse going low provided that $\overline{CS}$ is also low. The leading edge of the $\overline{WE}$ pulse is used to latch the status of the address bus. $\overline{CS}$ if active (low) will also be latched. NOTE: $\overline{WE}$ is gated by $\overline{CS}$. If $\overline{CS}$ goes low after $\overline{WE}$, the Write Cycle will be initiated by $\overline{CS}$, and all timing will be referenced to that edge. $\overline{CS}$ and the Addresses will then be latched, and the cycle must be terminated by $\overline{WE}$ going high. The output bus if not already disabled will go to the high Z state t_{WEZ} after $\overline{WE}$. The latch signal, if at a logic high, will have no impact on the WRITE cycle. If latch is brought from a logic high to low prior to $\overline{WE}$ going active then the address inputs and $\overline{CS}$ will be latched. NOTE: The Latch control ($\overline{L}$) will latch $\overline{CS}$ independent of the state, whereas $\overline{WE}$ will latch $\overline{CS}$ only when in the low state. Once latched, $\overline{CS}$ and the address inputs may be removed after the required hold times have been met.

Data in must be valid t_{DSW} prior to the low-to-high transition of $\overline{WE}$. The Data in lines must remain stable for t_{DHW} after $\overline{WE}$ goes inactive. The write control of the MK 4118 disables the data out buffers during the write cycle; however, output enable ($\overline{OE}$) should be used to disable the data out buffers to prevent bus contention between the input data and data that would be output upon completion of the write cycle.

READ/MODIFY/WRITE CYCLE

The MK4118 READ/MODIFY/WRITE cycle is merely a combination of the READ and WRITE cycle operations. The asynchronous or synchronous READ cycle may be combined with the WRITE operation. The status of DATA OUT bus will follow the operation outlined in the READ MODE or WRITE MODE.