EPSON

SED1200F

Dot Matrix LCD Controller Driver

Wide Voltage Operation Products

- **1/8 or 1/16 Duty Dot Matrix Drive**
- **20 Character Simultaneous Display**
- **Built in Character Generator ROM and RAM**

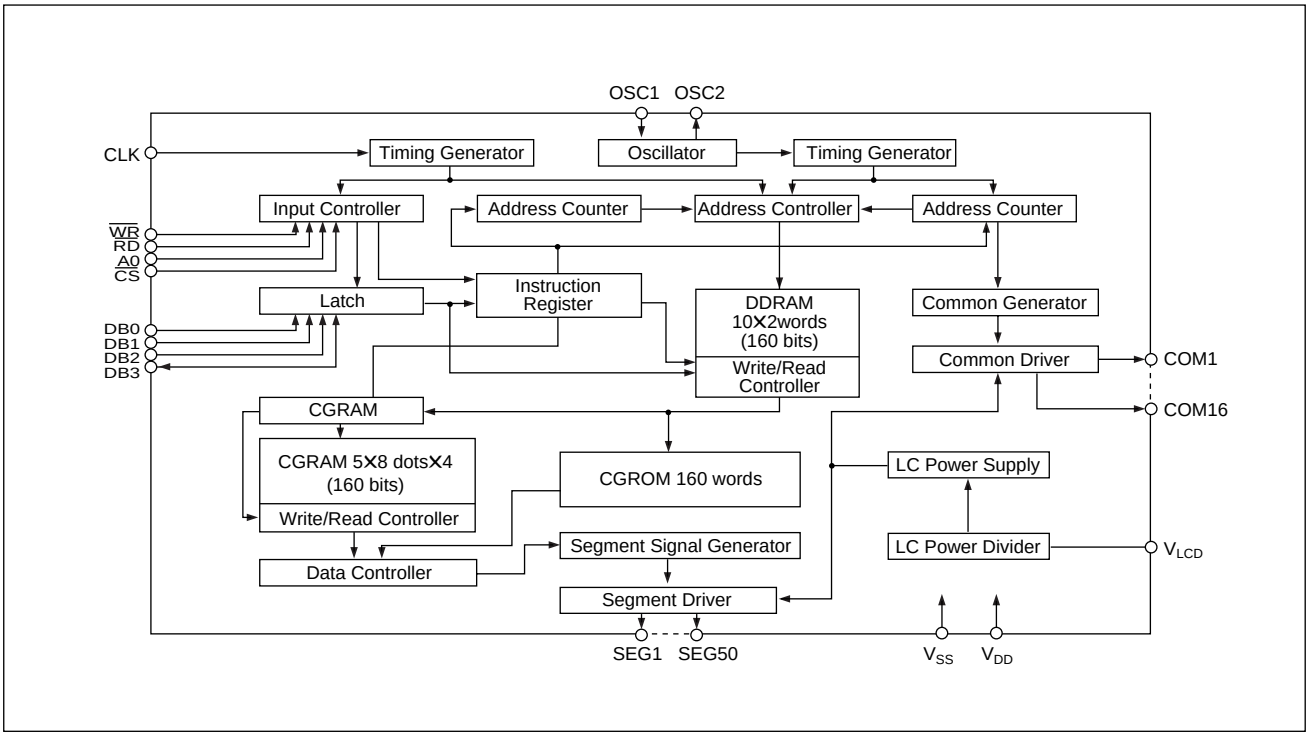
■ DESCRIPTION

The SED1200F is a dot matrix LCD controller/driver with a built in CG (character generator).
The circuit consists of a CG ROM which contains 160 different characters, 4 words CG RAM, 20 words display data RAM and logic functions to operate a 20 character display. Additional characters may be used by writing CG data to the 4 words CG RAM.
The device also contains the resistor array for the LCD power supply. The SED1200F is fabricated Silicon Gate CMOS process and features very low power dissipation. This makes the device very desirable for applications in hand held, portable and other battery powered instruments.

■ FEATURES

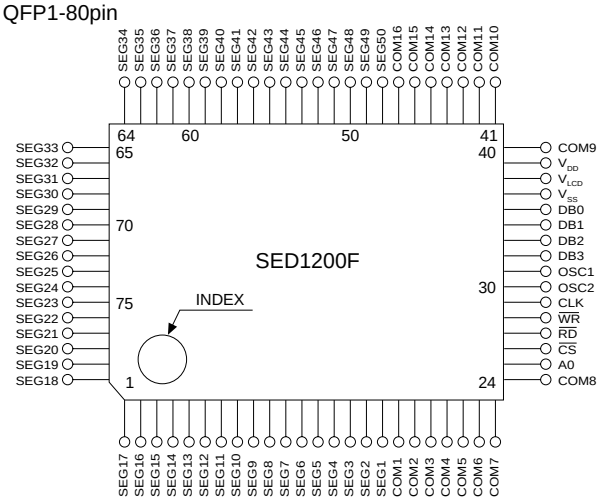
- 1/8 or 1/16 duty cycle dot matrix drive
- 20 character simultaneous display
- Built in character generator ROM and RAM
- Built in CR oscillator
- Built in resistor array for LCD power supply
- Compatible with 4 or 8 bit microprocessors
- 2 kinds of character font
- TTL Compatible
- 5×7+Cursor line or 558 character font
- Power supply Logic : 2.5V to 5.5V
  LCD : 3.5V to 5.5V
- Package ..... SED1200F : QFP1-80pin (plastic)
  SED1200D : Die form

■ BLOCK DIAGRAM



■ PIN CONFIGURATION

QFP1-80pin



■ PIN DESCRIPTION

Pin No.	Pin Name	I/O	Function
18 to 25 40 to 47	COM1 to COM16	O	LCD Common output
17 to 1 80 to 48	SEG1 to SEG 50	O	LCD Segment output
27	$\overline{CS}$	I	Chip select input (active "Low")
28	$\overline{RD}$	I	Read enable input (active "Low")
29	$\overline{WR}$	I	Write enable input (active "Low" to "High")
26	A0	I	"High" ; Set character code. "Low" ; Command
36 to 33	DB0 to DB3	I, I/O	Data input (except DB3 ; Data input/output)
30	CLK	I	Clock for command
32, 31	OSC1, OSC2	—	Connect oscillation resistor
39	V_{DD}	—	Supply voltage (+5V) for logic
37	V_{SS}	—	GND (0V)
38	V_{LCD}	—	Supply voltage for LCD

■ ABSOLUTE MAXIMUM RATINGS

(V_{SS} = 0V)

Rating	Symbol	Value	Unit
Supply voltage (1)	V_{DD}	–0.3 to+7.0	V
Supply voltage (2)	V_{LCD}	V_{DD}–7.0 to V_{DD}+0.3	V
Input voltage	V_I	–0.3 to V_{DD}+0.3	V
Output voltage	V_O	–0.3 to V_{DD}+0.3	V
Operating temperature	T_{opr}	–10 to+70	°C
Storage temperature	T_{stg}	–65 to+150	°C

■ ELECTRICAL CHARACTERISTICS

● AC Characteristics (Read cycle)

(V_{DD} = 5V±10%, V_{SS} = 0V, Ta = –10 to+70°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
A0 setup time to $\overline{RD}$	t_{AR}		0	—	—	ns
$\overline{CS}$ setup time to $\overline{RD}$	t_{CR}		0	—	—	ns
Output delay time from $\overline{RD}$	t_{RD}		—	—	250	ns
A0 hold time after $\overline{RD}$	t_{RA}		20	—	—	ns
$\overline{CS}$ hold time after $\overline{RD}$	t_{RC}		20	—	—	ns
Data hold time	t_{RH}		10	—	—	ns
Read pulse width	t_{RP}		350	—	—	ns
Input fall time	t_{HL}		—	—	50	ns
Input rise time	t_{LH}		—	—	50	ns

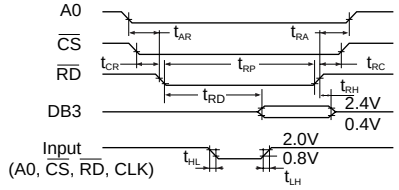
● AC Characteristics (Write cycle)

(V_{DD} = 5V±10%, V_{SS} = 0V, Ta = –10 to+70°C)

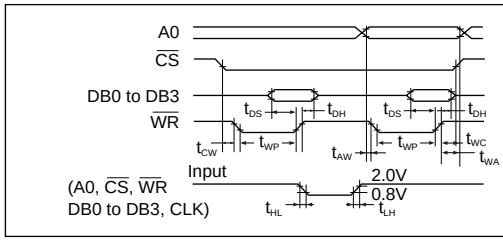
Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
A0 setup time to $\overline{WR}$	t_{AW}		0	—	—	ns
$\overline{CS}$ setup time to $\overline{WR}$	t_{CW}		0	—	—	ns
Data setup time	t_{DS}		120	—	—	ns
A0 hold time after $\overline{WR}$	t_{WA}		20	—	—	ns
$\overline{CS}$ hold time afrer $\overline{WR}$	t_{WC}		20	—	—	ns
Data hold time	t_{DH}		20	—	—	ns
Write pulse width	t_{WP}		200	—	—	ns
Input fall time	t_{HL}		—	—	50	ns
Input rise time	t_{LH}		—	—	50	ns

● Timing Chart

(Read cycle)



(Write cycle)



● DC Characteristics (V_{DD} = 5V)

(V_{SS} = 0V, Ta = –10 to +70°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Logic operating voltage	V_{DD}		4.5	5	5.5	V
LCD operating voltage	V_{LCD}		V_{DD}–5.5	—	V_{DD}–4	V
Resistor for oscillator	R_f	V_{DD} = 5V, f_{OSC} = 100kHz	240	310	380	kΩ
Input voltage; High (1)	V_{IH1}	V_{DD} = 4.5 to 5.5V ∗1	2.0	—	V_{DD}	V
Input voltage; Low (1)	V_{IL1}	V_{DD} = 4.5 to 5.5V ∗1	0	—	0.8	V
Input leakage current; High	I_{LIH}	V_{DD} = 5.5V, V_{IH} = 5.5V ∗2	—	—	1.0	µA
Input leakage current; Low	I_{LIL}	V_{DD} = 5.5V, V_{IL} = 0V ∗2	—	—	1.0	µA
Input voltage; High (2)	V_{IH2}	V_{DD} = 4.5 to 5.5V ∗3	0.8V_{DD}	V_{DD}	V_{DD}	V
Input voltage; Low (2)	V_{IL2}	V_{DD} = 4.5 to 5.5V ∗3	0	0	0.2V_{DD}	V
Output current; High	I_{OH}	V_{DD} = 5V, V_{OH} = 2.4V ∗4	1.0	—	—	mA
Output current; Low	I_{OL}	V_{DD} = 5V, V_{OL} = 0.4V ∗4	1.6	—	—	mA
Input pull up current	I_{IPU}	V_{IL} = 0V, V_{DD} = 5V ∗5	3	10	30	µA
Resistor as power divider	R_d		30	130	300	kΩ
Operating frequency (1)	f_{OSC}	V_{DD} = 4.5 to 5.5V	—	100	300	kHz
Operating frequency (2)	CLK	V_{DD} = 4.5 to 5.5V	—	—	3.2	MHz
Operating current	I_{DD}	V_{DD} = 5V, V_{LCD} = 0V ∗6 f_{OSC} = 100kHz, CLK = 1MHz	—	80	150	µA
Command execution time	t_{COMD}		—	—	16/CLK (MHz)	µs
Common output current (1)	I I_{OH} V_{DDC} I	V_{DD} = 4.5V	20	—	—	µA
Common output current (2)	I I_{OL} V_{LCDC} I	V_{LCD} = 1.0V	20	—	—	µA
Common output current (3)	I I_{OL} V_{L1C} I	1/16 duty drive	8	—	—	µA
Common output current (4)	I I_{OL} VL4C I	Voltage drop by 0.5V	8	—	—	µA
Segment output current (1)	I I_{OL} VDDS I	When one terminal is measured,	12	—	—	µA
Segment output current (2)	I I_{OL} VLCDS I	the others are open.	12	—	—	µA
Segment output current (3)	I I_{OL} VL2S I		4	—	—	µA
Segment output current (4)	I I_{OL} VL3S I		4	—	—	µA

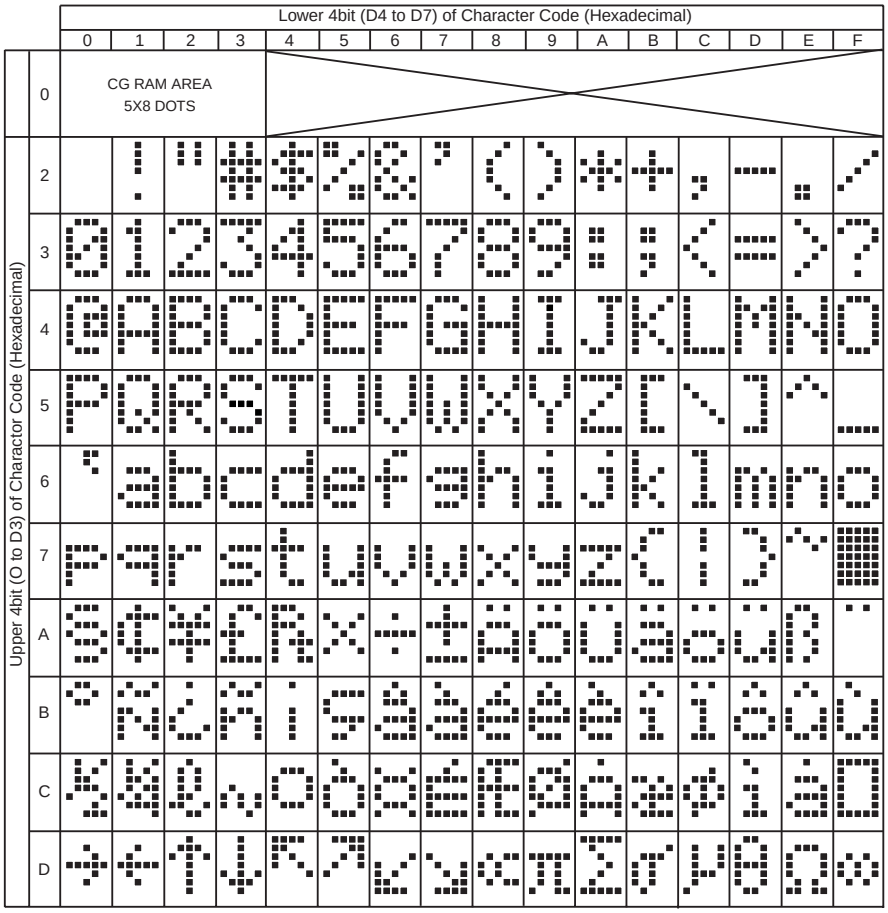
∗1. Terminal: $\overline{CS}$, $\overline{RD}$, $\overline{WR}$, A0, DB0 to DB3, CLK
∗2. Terminal: CLK, OSC1, DB0 to DB3
∗3. Terminal: OSC1 (for external clock)
∗4. Terminal: DB3
∗5. Terminal: $\overline{CS}$, $\overline{RD}$ $\overline{WR}$, A0
∗6. $\overline{CS}$ = $\overline{RD}$ = $\overline{WR}$ = A0 = 5.0V (open output terminals)

● Display Command

Command Name		$\overline{CS}$	$\overline{WR}$	$\overline{RD}$	AO	1st input DB3 (D7)	DB2 (D6)	DB1 (D5)	DB0 (D4)	2nd input DB3 (D3)	DB2 (D2)	DB1 (D1)	DB0 (D0)	Note
SET CURSOR DIRECTION		0	0	1	0	0	0	0	0	0	1	0	D/I	D0 = 1 : Decrement D0 = 0 : Increment
CURSOR ADDRESS–1/+1		0	0	1	0	0	0	0	0	0	1	1	–1/+1	D0 = 1 : –1 D0 = 0 : +1
CURSORFONT SELECT		0	0	1	0	0	0	0	0	1	0	0	A/U	D0 = 1 : All dots blinking D0 = 0 : Under line
CURSOR BLINK ON/OFF		0	0	1	0	0	0	0	0	1	0	1	ON/OFF	D0 = 1 : ON D0 = 0 : OFF
DISPLAY ON/OFF		0	0	1	0	0	0	0	0	1	1	0	ON/OFF	D0 = 1 : ON D0 = 0 : OFF
CURSOR ON/OFF		0	0	1	0	0	0	0	0	1	1	1	ON/OFF	D0 = 1 : ON D0 = 0 : OFF
SYSTEM RESET		0	0	1	0	0	0	0	1	0	0	0	0	Except data RAM and CGRAM
LINE SELECT		0	0	1	0	0	0	0	1	0	0	1	2/1	D0 = 1 : 2 line display (1/16 duty) D0 = 0 : 1 line display (1/8 duty)
SET CURSOR ADDRESS	1st LINE	0	0	1	0	1	0	(N figure—1)B						
	2nd LINE	0	0	1	0	1	1	(N figure—1)B						
SET CHARACTER CODE		0	0	1	1	(CHARACTER CODE)								
BUSY FLAG CHECK		0	1	0	0	BF	∗	∗	∗	BF	∗	∗	∗	D7 (D3 = 1 : Busy D7 (D3 = 0 : Not Busy
SET CGRAM ADDRESS		0	0	1	0	0	0	1	0	(Set lower address)				
SET CGRAM DATA		0	0	1	0	0	1	0	(Set CGRAM data)					

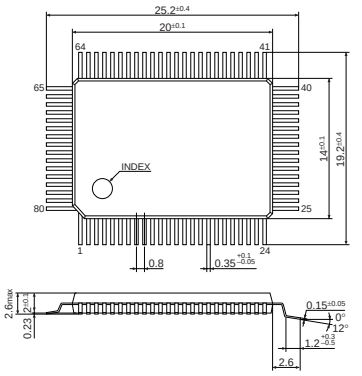
∗ = High impedance
Note: Misoperation may be caused when any command other than that listed in the above table is inputted.

■ CHARACTER CODE MAP (SED1200F$_{OB}$)



■ PACKAGE DIMENSIONS

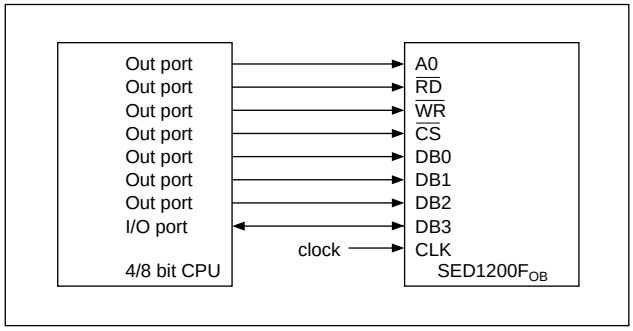
Plastic QFP1-80pin



Unit: mm

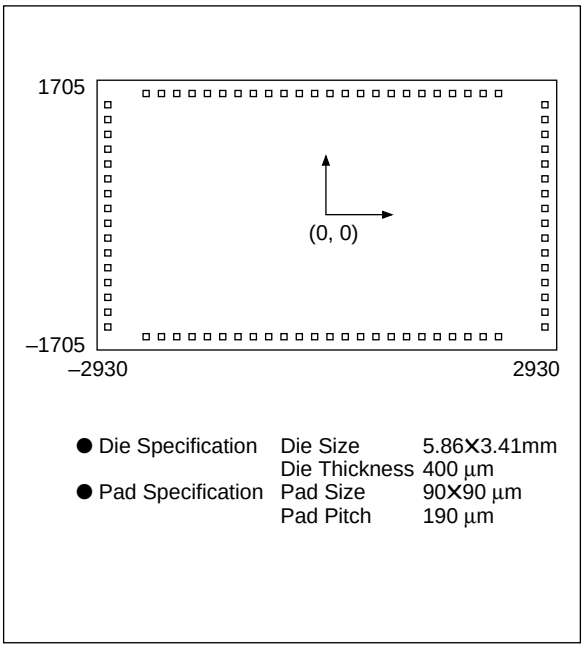
■ CPU INTERFACE

The SED1200F can connect to the address bus or the data bus directly or alternatively, a peripheral interface unit. An example is shown below.



■ DIE SPECIFICATION

● PAD LAYOUT



● Die Specification — Die Size 5.86×3.41mm; Die Thickness 400 μm

● Pad Specification — Pad Size 90×90 μm; Pad Pitch 190 μm

● PAD COORDINATION

unit : μm

Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y
1	SEG17	2123	1552	41	COM10	–2220	–1552
2	SEG16	1932	1552	42	COM11	–2029	–1552
3	SEG15	1742	1552	43	COM12	–1839	–1552
4	SEG14	1551	1552	44	COM13	–1648	–1552
5	SEG13	1361	1552	45	COM14	–1458	–1552
6	SEG12	1170	1552	46	COM15	–1267	–1552
7	SEG11	980	1552	47	COM16	–1077	–1552
8	SEG10	789	1552	48	SEG50	–886	–1552
9	SEG9	599	1552	49	SEG49	–696	–1552
10	SEG8	408	1552	50	SEG48	–505	–1552
11	SEG7	218	1552	51	SEG47	–315	–1552
12	SEG6	27	1552	52	SEG46	–124	–1552
13	SEG5	–163	1552	53	SEG45	66	–1552
14	SEG4	–354	1552	54	SEG44	257	–1552
15	SEG3	–544	1552	55	SEG43	447	–1552
16	SEG2	–735	1552	56	SEG42	638	–1552
17	SEG1	–925	1552	57	SEG41	828	–1552
18	COM1	–1116	1552	58	SEG40	1019	–1552
19	COM2	–1306	1552	59	SEG39	1209	–1552
20	COM3	–1497	1552	60	SEG38	1400	–1552
21	COM4	–1687	1552	61	SEG37	1590	–1552
22	COM5	–1878	1552	62	SEG36	1781	–1552
23	COM6	–2068	1552	63	SEG35	1971	–1552
24	COM7	–2259	1552	64	SEG34	2162	–1552
25	COM8	–2778	1429	65	SEG33	2777	–1385
26	$\underline{A0}$	–2778	1238	66	SEG32	2777	–1195
27	$\underline{CS}$	–2778	1048	67	SEG31	2777	–1004
28	$\underline{RD}$	–2778	857	68	SEG30	2777	–814
29	$\overline{WR}$	–2778	667	69	SEG29	2777	–623
30	ø	–2778	476	70	SEG28	2777	–433
31	XD	–2778	286	71	SEG27	2777	–242
32	XG	–2778	95	72	SEG26	2777	–52
33	DB3	–2778	–95	73	SEG25	2777	139
34	DB2	–2778	–286	74	SEG24	2777	329
35	DB1	–2778	–476	75	SEG23	2777	520
36	DB0	–2778	–667	76	SEG22	2777	710
37	VSS	–2778	–857	77	SEG21	2777	901
38	VLCD	–2778	–1048	78	SEG20	2777	1091
39	VDD	–2778	–1238	79	SEG19	2777	1282
40	COM9	–2778	–1429	80	SEG18	2777	1472

Note: The origin of cordination is center of the die.

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SEIKO EPSON CORPORATION

ELECTRONIC DEVICES MARKETING DIVISION

Electronic Device Marketing Department
IC Marketing & Engineering Group
421-8, Hino, Hino-shi, Tokyo 191-8501, JAPAN
Phone: +81-(0)42-587-5816 Fax: +81-(0)42-587-5624

ED International Marketing Department I (Europe & U.S.A.)
421-8, Hino, Hino-shi, Tokyo 191-8501, JAPAN
Phone: +81-(0)42-587-5812 Fax: +81-(0)42-587-5564

ED International Marketing Department II (Asia)
421-8, Hino, Hino-shi, Tokyo 191-8501, JAPAN
Phone: +81-(0)42-587-5814 Fax: +81-(0)42-587-5110

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http://www.epson.co.jp

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