SED1200 Series
LCD Controller/Drivers

Technical Manual

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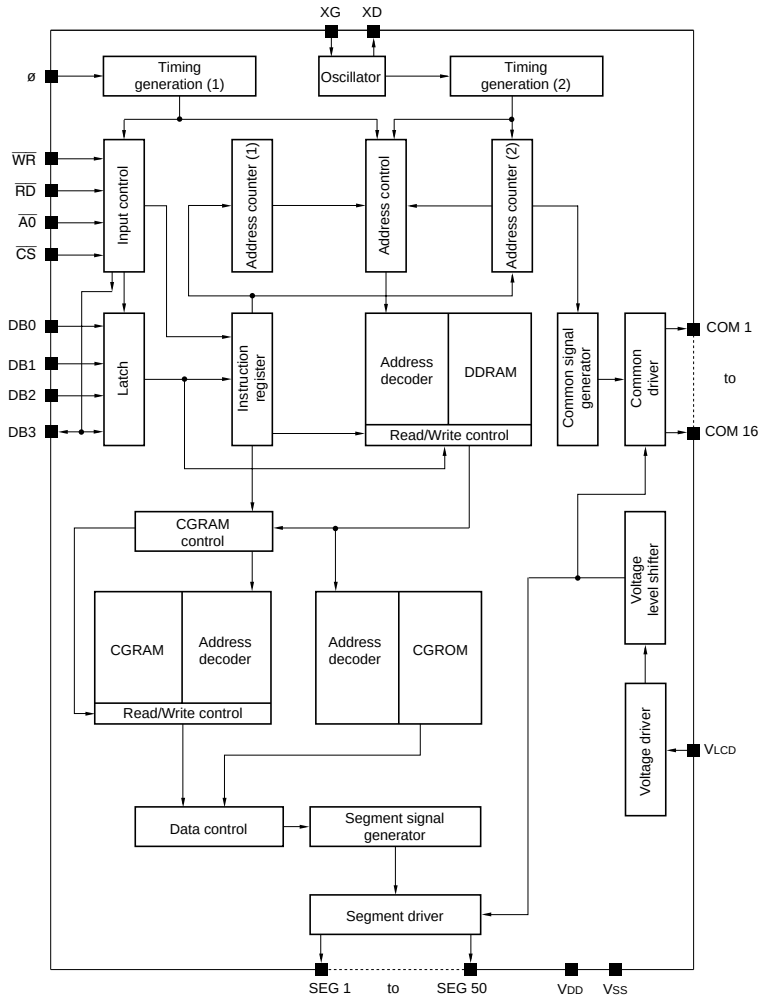
OVERVIEW

The SED1200 is a Liquid Crystal Display (LCD) character display controller-driver, capable of directly driving displays as large as 2 lines of 10 5×8 pixel characters, with a minimum of external components.
The SED1200 has an internal character generator (CG) consisting of 160 JIS ASCII characters in ROM and four user definable characters in RAM. The internal CG, a versatile set of cursor and display control commands, mean that the system CPU is only responsible for the display data and commands, and not for the LCD display itself.

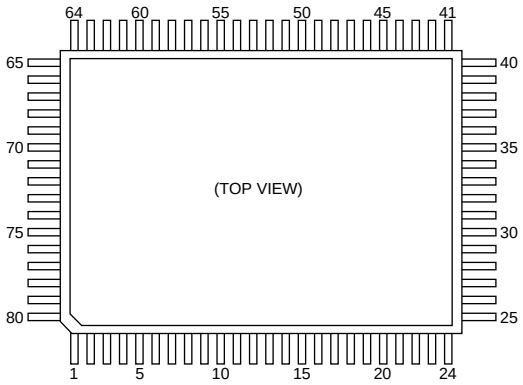
FEATURES

- Internal display RAM to hold 20 8-bit character codes.
- Internal character generator
  - CGROM: 160 JIS ASCII characters.
  - CGRAM: 4 user programmable 5×8 pixel characters
  - Font: 5×7 pixel characters plus the underline cursor.
  - JIS character set using SED1200F0A/SED1200D0A
  - ASCII character set using SED1200F0B/SED1200D0B
- Internal LCD driver circuitry
  - 50 segment driver lines
  - 16 common driver lines
  - Total size: Two lines of 10 characters each (maximum). One line of 20 characters (LCD panel dependent)
- CPU interface
  - 4-bit CPU data bus
  - 13 display control commands
- Low external component count
  - Built in RC oscillator (using one external feedback resistor)
  - Built in LCD driver voltage-divider network.
- Implemented using low power CMOS technology
  - TTL compatible CPU interface
- Power supply
  - Logic: 2.5 V to 5.5 V
  - LCD: 3.5 V to 5.5 V
- 80 pin QFP package SED1200F and chip (SED1200D)

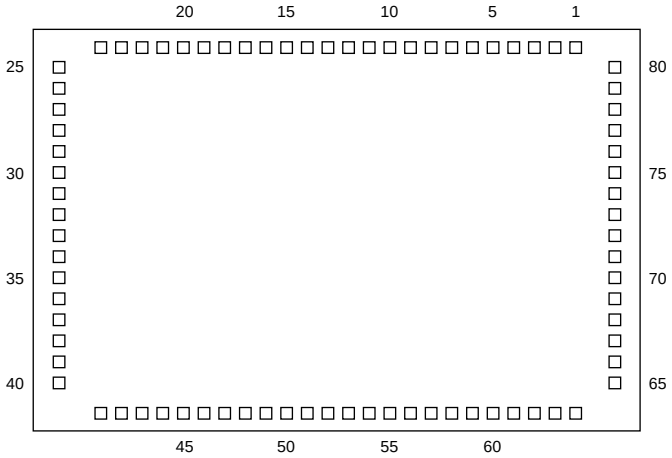
BLOCK DIAGRAM



PINOUT



SED1200F Package Outline



SED1200D Die Outline

TABLE 1. SED1200 Pinout

No.	NAME	No.	NAME	No.	NAME	No.	NAME
1	SEG17	21	COM4	41	COM10	61	SEG37
2	SEG16	22	COM5	42	COM11	62	SEG36
3	SEG15	23	COM6	43	COM12	63	SEG35
4	SEG14	24	COM7	44	COM13	64	SEG34
5	SEG13	25	COM8	45	COM14	65	SEG33
6	SEG12	26	A0	46	COM15	66	SEG32
7	SEG11	27	$\overline{CS}$	47	COM16	67	SEG31
8	SEG10	28	$\overline{RD}$	48	SEG50	68	SEG30
9	SEG9	29	$\overline{WR}$	49	SEG49	69	SEG29
10	SEG8	30	Φ	50	SEG48	70	SEG28
11	SEG7	31	X_D	51	SEG47	71	SEG27
12	SEG6	32	X_G	52	SEG46	72	SEG26
13	SEG5	33	DB3	53	SEG45	73	SEG25
14	SEG4	34	DB2	54	SEG44	74	SEG24
15	SEG3	35	DB1	55	SEG43	75	SEG23
16	SEG2	36	DB0	56	SEG42	76	SEG22
17	SEG1	37	V_{SS}	57	SEG41	77	SEG21
18	COM1	38	V_{LCD}	58	SEG40	78	SEG20
19	COM2	39	V_{DD}	59	SEG39	79	SEG19
20	COM3	40	COM9	60	SEG38	80	SEG18

PIN DESCRIPTION

CPU Interface

$\overline{CS}$ Active low chip select input.
$\overline{RD}$ Active low read enable input.
$\overline{WR}$ Active low write strobe.
A0 Selects between instruction and display data access.
A0 = H: Display data
A0 = L: Instruction
D0–D2 Active high CPU data inputs.
D3 Active high CPU data input/output.
Φ Clock input for command execution.

LCD Interface

COM1–COM16 LCD common driver outputs.
SEG1–SEG50 LCD segment driver outputs.

Oscillator

OSC1, OSC2 Terminals for the oscillator external feedback resistor, Rf. If an externally generated clock is used, it is connected to OSC1; OSC2 is left open.

Power Supply

V_{DD} Logic power supply
V_{LCD} LCD power supply
V_{SS} System ground (0 V).

COMMAND DESCRIPTION

Command Summary

TABLE 2. SED1200 Command Summary

COMMAND NAME	$\overline{CS}$	$\overline{WR}$	$\overline{RD}$	$\overline{A0}$	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
SET CURSOR DIRECTION	0	0	1	0	0	0	0	0	0	1	0	D/I	D0 = 1 ... Decrement D0 = 0 ... Increment
CURSOR ADDRESS –1/+1	0	0	1	0	0	0	0	0	0	1	1	–1/+1	D0 = 1 ... Cursor address –1 D0 = 0 ... Cursor address +1
CURSOR FONT SELECT	0	0	1	0	0	0	0	0	1	0	0	A/U	D0 = 1 ... All dots blinking D0 = 0 ... Underline
CURSOR BLINK ON/OFF	0	0	1	0	0	0	0	0	1	0	1	ON/OFF	D0 = 1 ... ON D0 = 0 ... OFF
DISPLAY ON/OFF	0	0	1	0	0	0	0	0	1	1	0	ON/OFF	D0 = 1 ... ON D0 = 0 ... OFF
CURSOR ON/OFF	0	0	1	0	0	0	0	0	1	1	1	ON/OFF	D0 = 1 ... ON D0 = 0 ... OFF
SYSTEM RESET	0	0	1	0	0	0	0	1	0	0	0	0	Data RAM & CGRAM are not affected
LINE SELECT	0	0	1	0	0	0	0	1	0	0	1	2/1	D0 =1 ... 2 line display (1/16 duty) D0 = 0 ... 1 line display (1/8 duty)
SET CGRAM ADDRESS	0	0	1	0	0	0	1	0	(LOWER ADDRESS)				Upper address fixed at 0H
SET CGRAM DATA	0	0	1	0	0	1	0	(CGRAM DATA)					
SET CURSOR ADDRESS	0	0	1	0	1	2nd/1st (N DIGIT-1)							D6 = 1 ... 2nd line N digit address D6 = 0 ... 1st line N digit address
SET CHARACTER CODE	0	0	1	1	(CHARACTER CODE)								
BUSY FLAG CHECK	0	1	0	0	BF	*	*	*	BF	*	*	*	High impedance

Write Commands

SET CURSOR DIRECTION

A0 = 0

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	1	0	D

Sets the way in which the cursor address register changes as character data is written to the SED1200 by the CPU, and hence the direction of cursor movement.

D = 0: Address register increment direction
D = 1: Address register decrement direction

CURSOR ADDRESS –1/+1

A0 = 0

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	1	1	D

Adds one to, or subtracts one from, the current contents of the cursor address register, and hence moves the cursor.

D = 0: ADDRESS = ADDRESS + 1
D = 1: ADDRESS = ADDRESS – 1

CURSOR FONT SELECT

A0 = 0

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	0	0	D

D = 0: Underline cursor
D = 1: All dots blinking

CURSOR BLINK ON/OFF

A0 = 0

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	0	1	D

Controls flashing of the underline cursor.
D = 0: Flashing stopped
D = 1: Cursor flashing

DISPLAY ON/OFF

A0 = 0

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	1	0	D

D = 0: Display Blanked
D = 1: Display on
Note: This command does not affect the contents of the display data RAM.

CURSOR ON/OFF

A0 = 0

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	1	1	D

Controls the display of the cursor.
D = 0: Cursor off.
D = 1: Cursor on.

SYSTEM RESET

A0 = 0

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	0	0	0

Initializes the SED1200 to the following defaults.
1. CURSOR DIRECTION: Increment
2. CURSOR FONT: Underline
3. CURSOR BLINK: Off
4. DISPLAY: Off
5. CURSOR: Off
6. LINE SELECT: One line display
7. CURSOR ADDRESS: Address 0 (Line 1, character 0)

Note: SYSTEM RESET does not affect the contents of the display data RAM, or the CGRAM.

LINE SELECT

A0 = 0

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	0	1	D

Selects the number of displayed lines, and hence the LCD drive duty cycle.
D = 0: 1 line display (1/8 duty cycle)
D = 1: 2 line display (1/16 duty cycle)
Note: The number of lines which can be displayed depends on the LCD panel used.

SET CURSOR ADDRESS

A0 = 0

D7	D6	D5	D4	D3	D2	D1	D0
1	L	P_5	P_4	P_3	P_2	P_1	P_0

Presets the contents of the cursor address register, and hence the position of the cursor.
L = 0: Line 1 select
L = 1: Line 2 select
P_5–P_0: Position of character in selected line.

SET CHARACTER CODE

A0 = 1

D7	D6	D5	D4	D3	D2	D1	D0
C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0

Writes the character code given by C_7–C_0 into the character data RAM at the location pointed to by the contents of the cursor address register. The contents of the cursor address register are then modified as specified by the last SET CURSOR DIRECTION instruction.

SET CGRAM ADDRESS

A0 = 0

D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	*	*	A_1	A_0

Presets the contents of the CGRAM address register to the position of one of the four user definable characters. The address is specified by A_1 and A_0.

SET CGRAM DATA

Loads the bit pattern D_4–D_0 into the CGRAM location specified by the current contents of the CGRAM address register. The contents of the CGRAM Address Register are incremented following each write of a SET CGRAM DATA instruction by the CPU.

A0 = 0

D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	D_4	D_3	D_2	D_1	D_0

See section 4.3, Loading CGRAM.

Read Commands

BUSY FLAG CHECK

Reading yields the status of the SED1200F.

A0 = 0

D7	D6	D5	D4	D3	D2	D1	D0
BF	*	*	*	BF	*	*	*

BF = 0: SED1200 READY
BF = 1: SED1200 BUSY
Bits D2–D0 are tristate during reads of the Busy Flag.

SPECIFICATIONS

Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Supply voltage (1)	V_{DD}	–0.3 to +7.0	V
Supply voltage (2)	V_{LCD}	V_{DD}–7.0 to V_{DD}+0.3	V
Input voltage	V_{IN}	–0.3 to V_{DD}+0.3	V
Output voltage	V_{OUT}	–0.3 to V_{DD}+0.3	V
Operating temperature	T_{opr}	–10 to +70	°C
Storage temperature	T_{stg}	–40 to +125	°C
Soldering temperature and time	T_{sol}	260, 10	°C, s

Electrical Specifications

DC Characteristics

V_{DD} = 5 V

V_{SS} = 0 V, T_a = –10 to +70°C

Parameter	Symbol	Condition	Rating min	Rating typ	Rating max	Unit	Pin
Logic supply voltage	V_{DD}		4.5	5.0	5.5	V	V_{DD}
Liquid crystal display supply voltage	V_{LCD}		V_{DD}–5.5	—	V_{DD}–3.5	V	V_{LCD}
Oscillator feedback resistor	R_f	V_{DD} = 5.0 V, f_{OSC} = 100 kHz	240	310	380	kΩ	X_G, X_D
Operating frequency (1) oscillator or external clock frequency	f_{OSC}	V_{DD} = 4.5 to 5.5 V	—	100	300	kHz	X_G, X_D
Operating frequency (2)	Φ	V_{DD} = 4.5 to 5.5 V	—	—	3.2	MHz	Φ
External clock duty		V_{DD} = 4.5 to 5.5 V	45	50	55	%	X_G, Φ
External clock rise time	t_r	V_{DD} = 4.5 to 5.5 V	—	—	50	ns	X_G, Φ
External clock fall time	t_f	V_{DD} = 4.5 to 5.5 V	—	—	50	ns	X_G, Φ
H-level input voltage (1)	V_{IH1}	V_{DD} = 4.5 to 5.5 V	2.0	—	V_{DD}	V	$\overline{CS}$, $\overline{RD}$, $\overline{WR}$, DB0 to DB3, Φ
L-level input voltage (1)	V_{IL1}	V_{DD} = 4.5 to 5.5 V	0	—	0.8	V	
H-level input voltage (2)	V_{IH2}	V_{DD} = 4.5 to 5.5 V	0.8 V_{DD}	V_{DD}	V_{DD}	V	X_G
L-level input voltage (2)	V_{IL2}	V_{DD} = 4.5 to 5.5 V	0	0	0.2 V_{DD}	V	
H-level input leakage current	I_{LIH}	V_{DD} = 5.5 V, V_{IH} = 5.5 V	—	—	|–1.0|	µA	Φ, X_G, DB0 to DB3
L-level input leakage current	I_{LIL}	V_{DD} = 5.5 V, V_{IL} = 0 V	—	—	1.0	µA	
Input pull-up current	I_{IPU}	V_{DD} = 5.0 V, V_{IL} = 0 V	3.0	10	30	µA	$\overline{CS}$, $\overline{RD}$, $\overline{WR}$, A0
H-level output current	I_{OH}	V_{DD} = 4.5 to 5.5 V, V_{OH} = 2.4 V	|–1.0|	—	—	mA	DB3
L-level output current	I_{OL}	V_{DD} = 5.5 V, V_{OL} = 0.4 V	1.6	—	—	mA	
Common driver output current (1)	I_{OH}	V_{DD} level; V_{DD}=4.5 V, V_{LCD}=1.0 V, Voltage-divider resistor in low impedance state. 1/16 duty, 0.5 V voltage drop, Measured on one pin with other pins open circuit.	|–20|	—	—	µA	COM1 to COM16
Common driver output current (2)	I_{OL}	V_{LCD} level	20	—	—	µA	COM1 to COM16
Common driver output current (3)	I_{OL}	V_{L1} level	|±8|	—	—	µA	COM1 to COM16
Common driver output current (4)	I_{OL}	V_{L4} level	|±8|	—	—	µA	COM1 to COM16
Segment driver output current (1)	I_{OH}	V_{DD} level	|–12|	—	—	µA	SEG1 to SEG50
Segment driver output current (2)	I_{OL}	V_{LCD} level	12	—	—	µA	SEG1 to SEG50
Segment driver output current (3)	I_{OL}	V_{L2} level	|±4|	—	—	µA	SEG1 to SEG50
Segment driver output current (4)	I_{OL}	V_{L3} level	|±4|	—	—	µA	SEG1 to SEG50
Voltage-divider resistor (1)	R_{d1}	Normal conditions	30	130	300	kΩ	
Voltage-divider resistor (2)	R_{d2}	Low impedance state	3.0	13	30	kΩ	
Voltage-divider resistor low impedance duty	t_{Rd1}/t_{Rd2}	1/8 Duty	—	11/400	—	—	
		1/16 Duty	—	11/200	—	—	
Command execution time	t_{comd}	From $\overline{WR}$ rising edge to the end of internal processing	—	—	16/Φ (MHz)	µs	
Average operating current	I_{DD}	V_{DD} = 5.0 V, V_{LCD} = 0 V, f_{OSC} = 100 kHz, Φ = 1 MHz, $\overline{CS}$ = $\overline{RD}$ = $\overline{WR}$ = A0 = 5.0 V, output open	—	80	150	µA	V_{DD}

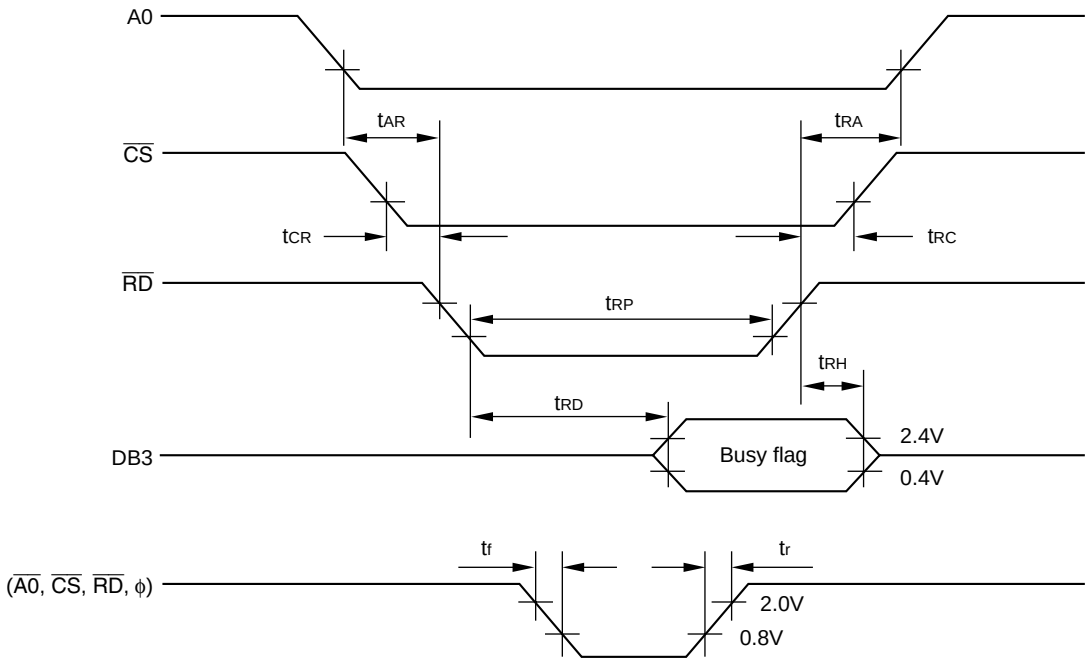
V_{DD} = 3 V

V_{SS} = 0 V, Ta = –10 to 70°C

Parameter	Symbol	Condition	Rating min	Rating typ	Rating max	Unit	Pin
Logic supply voltage	V_{DD}		2.5	3.5	4.5	V	V_{DD}
Liquid crystal display supply voltage	V_{LCD}		V_{DD}–5.5	—	V_{DD}–3.5	V	V_{LCD}
Oscillator feedback resistor	R_f	V_{DD} = 3.0 V, f_{OSC} = 100 kHz	210	290	370	kΩ	X_G, X_D
Operating frequency (1) oscillator or external clock frequency	f_{OSC}	V_{DD} = 2.5 V	—	—	300	kHz	X_G, X_D
Operating frequency (2)	Φ	V_{DD} = 2.5 V	—	—	1.0	MHz	Φ
External clock duty		V_{DD} = 2.5v	—	50	—	%	OSC1, Φ
External clock rise time	t_r	V_{DD} = 2.5 V	—	—	50	ns	OSC1, Φ
External clock fall time	t_f	V_{DD} = 2.5 V	—	—	50	ns	OSC1, Φ
H-level input voltage (1)	V_{IH1}	V_{DD} = 2.5 V	0.8 V_{DD}	—	V_{DD}	V	$\overline{CS}$, $\overline{RD}$, $\overline{WR}$,
L-level input voltage (1)	V_{IL1}	V_{DD} = 2.5 V	0	—	0.2 V_{DD}	V	DB0 to DB3, Φ
H-level input voltage (2)	V_{IH2}	V_{DD} = 2.5V	0.8 V_{DD}	—	—	V	X_G
L-level input voltabe (2)	V_{IL2}	V_{DD} = 2.5 V	—	—	0.2 V_{DD}	V	
H-level input leakage current	I_{LIH}	V_{DD} = 4.5 V	—	—	|–1.0|	µA	Φ, X_G,
L-level input leakage current	I_{LIL}	V_{DD} = 4.5 V	—	—	1.0	µA	DB0 to DB3
Input pull-up current	I_{IPU}	V_{DD} = 3.5 V	1.0	4.0	15	µA	$\overline{CS}$, $\overline{RD}$, $\overline{WR}$, A0
H-level output current	I_{OH}	V_{DD} = 2.5 V, V_{OH} = 2.0 V	200	—	—	µA	DB3
L-level output current	I_{OL}	V_{DD} = 2.5 V, V_{OL} = 0.5 V	200	—	—	µA	
Common driver output current (1)	I_{OH}	V_{DD} level; V_{DD}–V_{LCD} = 3.5 V Voltage-divider resistor in low impedance state. 1/16 duty 0.5 V voltage drop Measured on one pin with other pins open circuit.	|-20|	—	—	µA	COM1 to COM16
Common driver output current (2)	I_{OL}	V_{LCD} level	20	—	—	µA	
Common driver output current (3)	I_{OL}	V_{L1} level	|±8|	—	—	µA	
Common driver output current (4)	I_{OL}	V_{L4} level	|±8|	—	—	µA	
Segment drivrer output current (1)	I_{OH}	V_{DD} level	|–12|	—	—	µA	SEG1 to SEG50
Segment drivrer output current (2)	I_{OL}	V_{LCD} level	12	—	—	µA	
Segment drivrer output current (3)	I_{OL}	V_{L2} level	|±4|	—	—	µA	
Segment drivrer output current (4)	I_{OL}	V_{L3} level	|±4|	—	—	µA	
Voltage-divider resistor (1)	R_{d1}	Normal conditions	—	130	—	kΩ	
Voltage-divider resistor (2)	R_{d2}	Low impedance state	—	13	—	kΩ	
Voltage-divider resistor low impedance duty	t_{Rd1}/t_{Rd2}	1/8 Duty	—	11/400	—	—	
		1/16 Duty	—	11/200	—	—	
Command execution time	t_{comd}	From $\overline{WR}$ rise time to the end of internal processing	—	—	16/Φ (MHz)	µs	
Average operating current	I_{DD}	V_{DD}–V_{SS} = 3.5 V V_{DD}–V_{LCD} = 1.5 V f_{OSC} = 100 kHz, Φ = 500 kHz $\overline{CS}$ = $\overline{RD}$ = $\overline{WR}$ = A0 = V_{DD}, output open	—	60	—	µA	V_{DD}

AC Characteristics

MPU Read Timing



V_{DD} = 4.5 to 5.5 V, Ta = –10 to 70°C.

Parameter	Symbol	Rating			Unit
		min	typ	max	
Setup time for A0 → $\overline{RD}$	t_{AR}	0	—	—	ns
Setup time for $\overline{CS}$ → $\overline{RD}$	t_{CR}	0	—	—	ns
$\overline{RD}$ delay output time	t_{RD}	—	—	250	ns
Hold time for $\overline{RD}$ → A0	t_{RA}	20	—	—	ns
Hold time for $\overline{RD}$ → $\overline{CS}$	t_{RC}	20	—	—	ns
Data hold time	t_{RH}	10	—	—	ns
Read pulsewidth	t_{RP}	350	—	—	ns
Input fall time	t_f	—	—	50	ns
Input rise time	t_r	—	—	50	ns

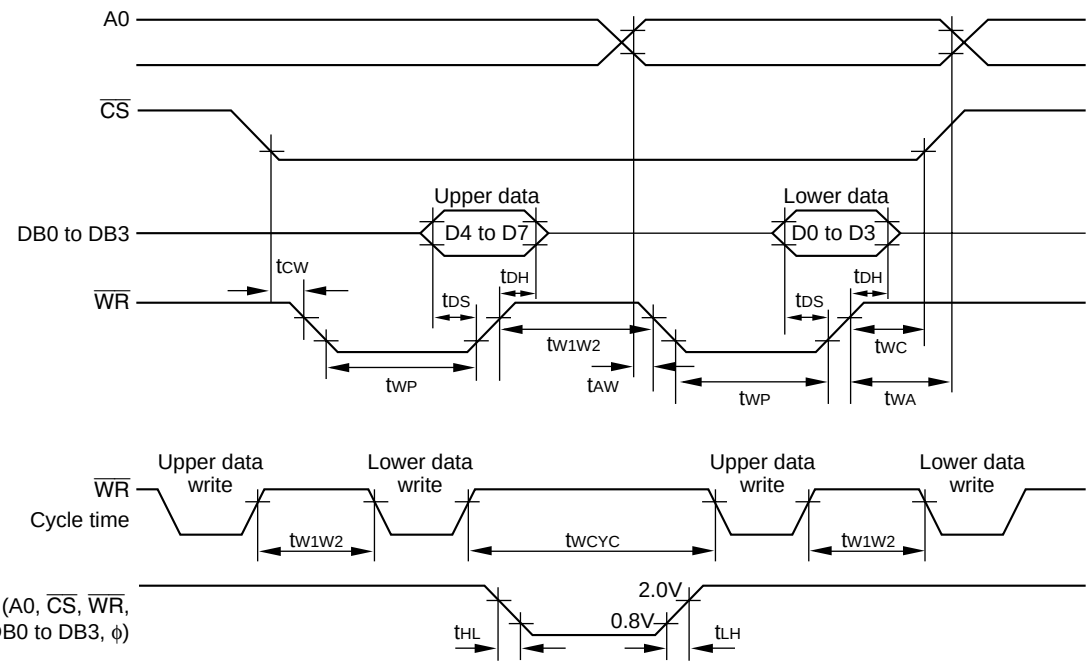
Note: Load on pin DB3 is C_L = 100 pF.

V_{DD} = 2.5 to 4.5 V, Ta = –10 to 70°C.

Parameter	Symbol	Rating			Unit
		min	typ	max	
Setup time for A0 → $\overline{RD}$	t_{AR}	0	—	—	ns
Setup time for $\overline{CS}$ → $\overline{RD}$	t_{CR}	0	—	—	ns
$\overline{RD}$ delay output time	t_{RD}	—	—	350	ns
Hold time for $\overline{RD}$ → A0	t_{RA}	0	—	—	ns
Hold time for $\overline{RD}$ → $\overline{CS}$	t_{RC}	0	—	—	ns
Data hold time	t_{RH}	10	—	—	ns
Read pulsewidth	t_{RP}	400	—	—	ns
Input fall time	t_f	—	—	50	ns
Input rise time	t_r	—	—	50	ns

Note: Load on pin DB3 is C_L = 100 pF.

MPU Write Timing



V_{DD} = 5 V, Ta = –10 to 70°C.

Parameter	Symbol	Rating			Unit
		min	typ	max	
A0 → $\overline{WR}$ setup time	t_{AW}	0	—	—	ns
$\overline{CS}$ → $\overline{WR}$ setup time	t_{CW}	0	—	—	ns
Data setup time	t_{DS}	120	—	—	ns
$\overline{WR}$ → A0 hold time	t_{WA}	20	—	—	ns
$\overline{WR}$ → $\overline{CS}$ hold time	t_{WC}	20	—	—	ns
Data hold time	t_{DH}	20	—	—	ns
Write pulsewidth	t_{WP}	200	—	—	ns
Upper write pulse rising edge to lower write pulse falling edge time.	t_{W1W2}	200	—	—	ns
Lower write pulse rising edge to upper write pulse falling edge time.	t_{WCYC}	16/Φ (MHz)	—	—	ns
Input fall time	t_f	—	—	50	ns
Input rise time	t_r	—	—	50	ns

V_{DD} = 3 V, Ta = –10 to 70°C.

Parameter	Symbol	Rating			Unit
		min	typ	max	
A0 → $\overline{WR}$ setup time	t_{AW}	0	—	—	ns
$\overline{CS}$ → $\overline{WR}$ setup time	t_{CW}	0	—	—	ns
Data setup time	t_{DS}	120	—	—	ns
$\overline{WR}$ → A0 hold time	t_{WA}	0	—	—	ns
$\overline{WR}$ → $\overline{CS}$ hold time	t_{WC}	0	—	—	ns
Data hold time	t_{DH}	100	—	—	ns
Write pulsewidth	t_{WP}	200	—	—	ns
Upper write pulse rising edge to lower write pulse falling edge time.	t_{W1W2}	200	—	—	ns
Lower write pulse rising edge to upper write pulse falling edge time.	t_{WCYC}	16/Φ (MHz)	—	—	ns
Input fall time	t_f	—	—	50	ns
Input rise time	t_r	—	—	50	ns

OPERATION

Data Input/Output

Because the command codes are 8-bits wide and the SED1200's data bus is only 4-bits wide, the command codes must be split into two nibbles (4-bits), which are written separately.

Nibble	High-order				Low-order			
Data Bus Bit	D3	D2	D1	D0	D3	D2	D1	D0
Command Bit	D7	D6	D5	D4	D3	D2	D1	D0

The high-order nibble is written first, and is latched internally by the SED1200. When the low-order nibble is written, the eight bits of data are shifted into either the character registers or the command register, depending on the level of A0 during the low-nibble write cycle.

When the busy flag is read, only one read cycle is required.

New commands must not be written to the SED1200 if the device is executing one currently, so the busy flag should be checked before commands are written. It is not necessary to check the busy flag between writes of the upper and lower nibbles of commands. If the busy flag is not going to be checked between writes of individual commands then the MPU must wait long enough to allow for command execution to complete. The maximum time taken by the SED1200 to execute a command is 16/Φ, where Φ is the system clock frequency.

System Initialization

Figure 1 is a flow chart of a possible SED1200 initialization sequence. Note that busy flag checks, and busy/wait loops have been omitted for the sake of brevity.

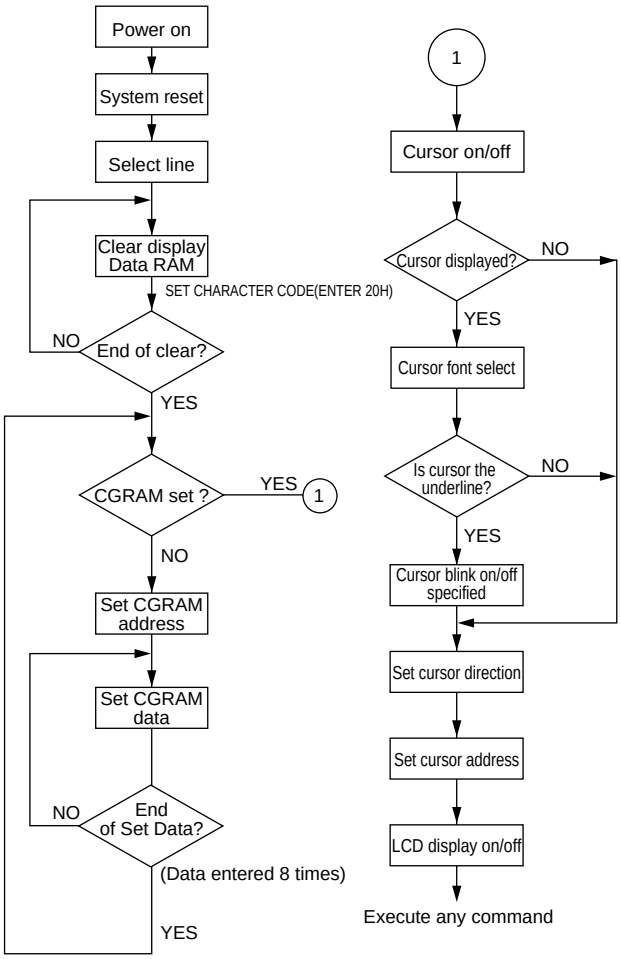


Figure 1. Initialization Flow Chart

Loading CGRAM

The character generator RAM is loaded with a character bit pattern using a combination of one SET CGRAM ADDRESS command and eight SET CGRAM DATA commands. For example, to load the character shown in figure 2 into the area of CGRAM corresponding to character code 01H, the sequence shown in table 3 is used.

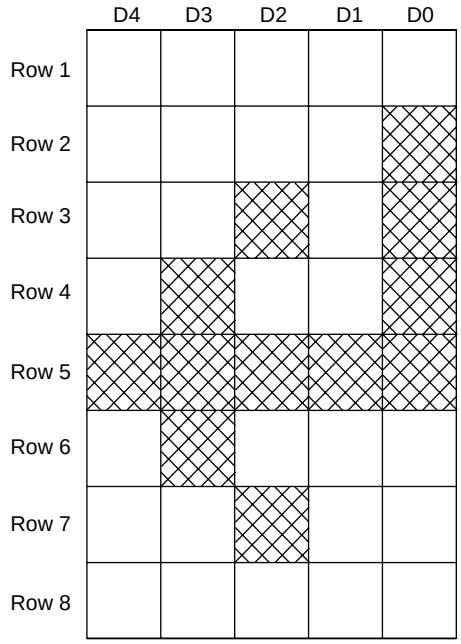


Figure 2. User Defined Character

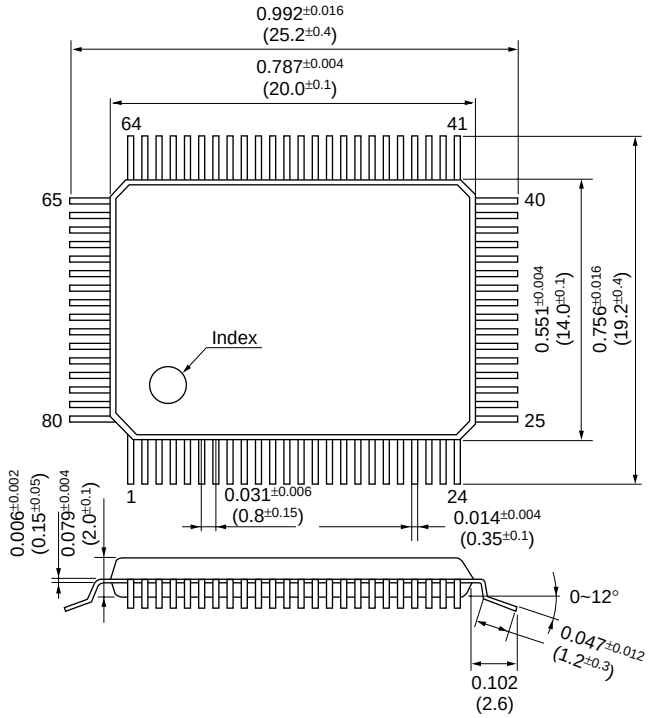
TABLE 3. Loading User Defined Character

Step	A0	$\overline{WR}$	Data	Action
1	0	0	21H	Set address of CGRAM 01
2	0	0	40H	Data for Row 1
3	0	0	41H	Data for Row 2
4	0	0	45H	Data for Row 3
5	0	0	49H	Data for Row 4
6	0	0	5FH	Data for Row 5
7	0	0	48H	Data for Row 6
8	0	0	44H	Data for Row 7
9	0	0	40H	Data for Row 8

Notes: 1. These steps do not include busy flag checks.
2. Row 8 maybe used by the underline cursor.

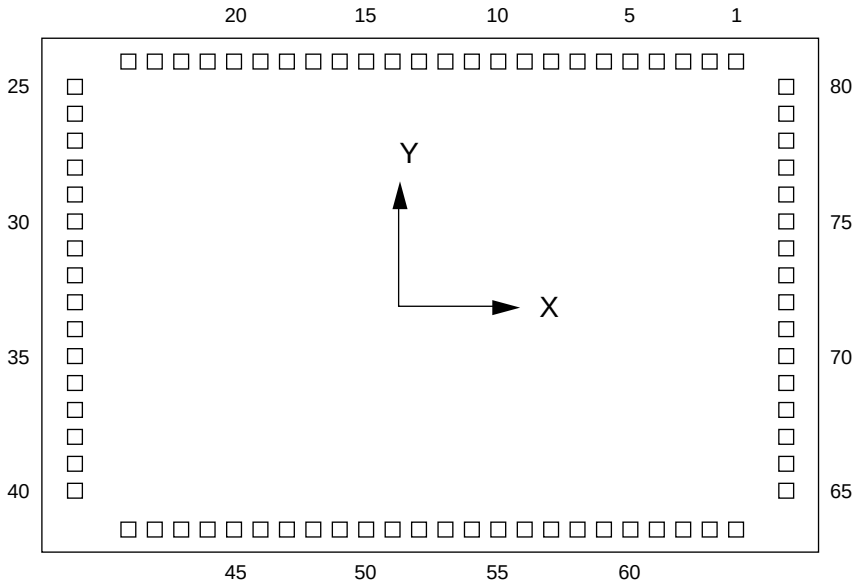
Mechanical Specifications

SED1200F Package Dimensions



SED1200D Package Dimensions

Chip size: 5.86 mm × 3.41 mm
Chip thickness: 0.40 mm ± 0.03 mm
Pad size: 0.90 mm × 0.90 mm
Pad pitch: 0.19 mm



Pad		X (μm)	Y (μm)
Number	Name		
1	SEG17	2123	1552
2	SEG16	1932	1552
3	SEG15	1742	1552
4	SEG14	1551	1552
5	SEG13	1361	1552
6	SEG12	1170	1552
7	SEG11	980	1552
8	SEG10	789	1552
9	SEG9	599	1552
10	SEG8	408	1552
11	SEG7	218	1552
12	SEG6	27	1552
13	SEG5	–163	1552
14	SEG4	–354	1552
15	SEG3	–544	1552
16	SEG2	–735	1552
17	SEG1	–925	1552
18	COM1	–1116	1552
19	COM2	–1306	1552
20	COM3	–1497	1552
21	COM4	–1687	1552
22	COM5	–1878	1552
23	COM6	–2068	1552
24	COM7	–2259	1552
25	COM8	–2778	1429
26	A0	–2778	1238
27	$\overline{CS}$	–2778	1048
28	$\overline{RD}$	–2778	857
29	$\overline{WR}$	–2778	667
30	Φ	–2778	476
31	OSC2	–2778	286
32	OSC1	–2778	95
33	D3	–2778	–95
34	D2	–2778	–286
35	D1	–2778	–476
36	D0	–2778	–667
37	V_{SS}	–2778	–857
38	V_{LCD}	–2778	–1048
39	V_{DD}	–2778	–1238
40	COM9	–2778	–1429

Pad		X (μm)	Y (μm)
Number	Name		
41	COM10	–2220	–1552
42	COM11	–2029	–1552
43	COM12	–1839	–1552
44	COM13	–1648	–1552
45	COM14	–1458	–1552
46	COM15	–1267	–1552
47	COM16	–1077	–1552
48	SEG50	–886	–1552
49	SEG49	–696	–1552
50	SEG48	–505	–1552
51	SEG47	–315	–1552
52	SEG46	–124	–1552
53	SEG45	66	–1552
54	SEG44	257	–1552
55	SEG43	447	–1552
56	SEG42	638	–1552
57	SEG41	828	–1552
58	SEG40	1019	–1552
59	SEG39	1209	–1552
60	SEG38	1400	–1552
61	SEG37	1590	–1552
62	SEG36	1781	–1552
63	SEG35	1971	–1552
64	SEG34	2162	–1552
65	SEG33	2777	–1385
66	SEG32	2777	–1195
67	SEG31	2777	–1004
68	SEG30	2777	–814
69	SEG29	2777	–623
70	SEG28	2777	–433
71	SEG27	2777	–242
72	SEG26	2777	–52
73	SEG25	2777	139
74	SEG24	2777	329
75	SEG23	2777	520
76	SEG22	2777	710
77	SEG21	2777	901
78	SEG20	2777	1091
79	SEG19	2777	1282
80	SEG18	2777	1472

APPLICATION NOTES

Display Oscillator

The SED1200 has an internal oscillator to generate the timing signals required for the LCD display.
If the internal oscillator is used, connect the feedback resistor Rf as shown in figure 3. The feedback resistor leads must be kept as short as possible to reduce stray capacitance and the possibility of crosstalk between the oscillator and adjoining signals.

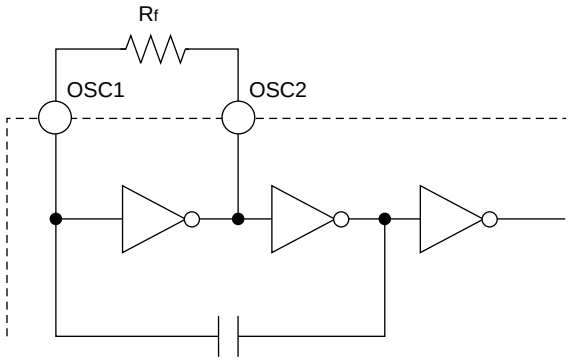


Figure 3. Using the Internal Oscillator

If an external clock is used, connect it to OSC1, as shown in figure 4.

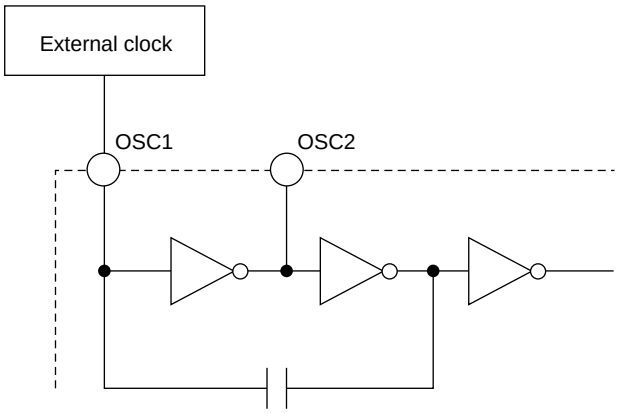


Figure 4. Using an External Clock

The relationship between the oscillator frequency and the LCD drive frame frequency is

$f_{FR} = f_{OSC}/1600$
For example if f_{OSC} = 100 kHz, f_{FR} = 62.5 Hz

Command Clock (Φ)

When the system MPU issues a command to the SED1200, the timing for the execution of the command is derived from Φ, the command clock. This would normally be the system MPU clock.
The maximum execution time for a command is 16/Φ. For example if Φ= 1 MHz, the maximum execution time for a command is 16 μs.

LCD Drive Waveforms

The SED1200 has an internal low source-impedance voltage-driver network, of the form shown in figure 5. The switches Swd are closed to switch the segment data.

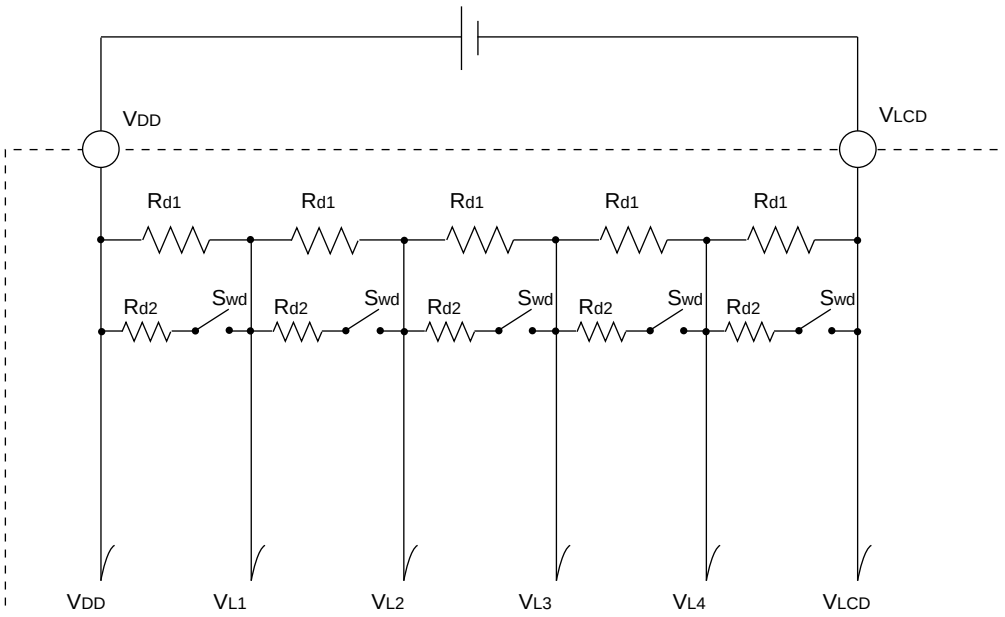
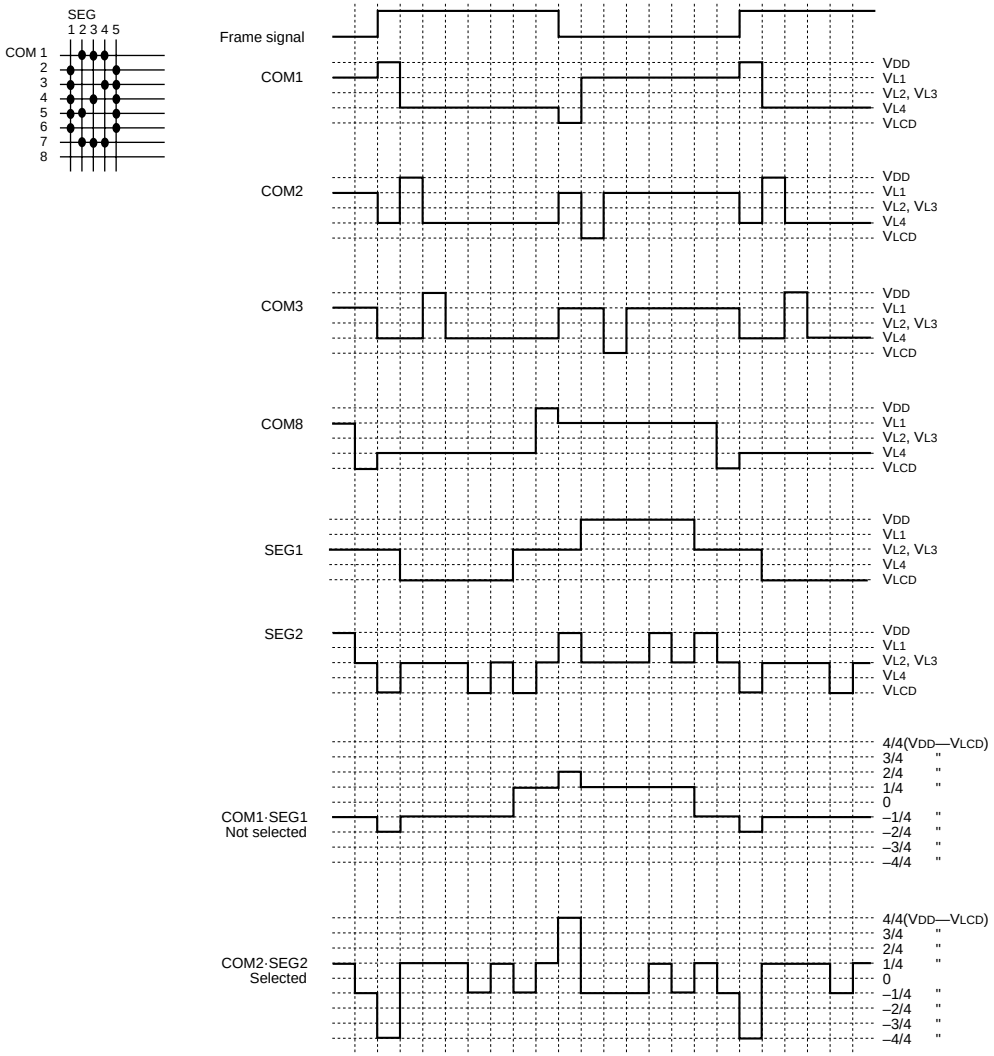
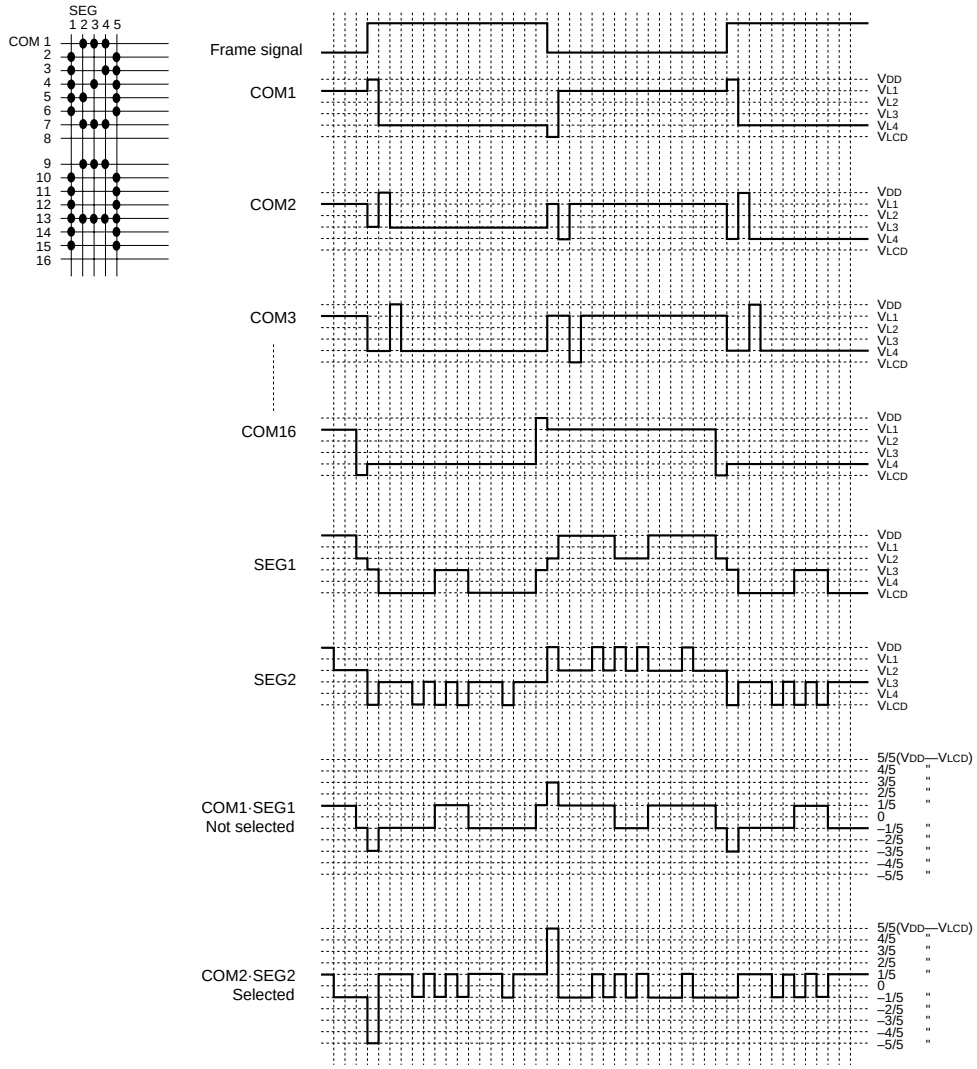


Figure 5. Internal Voltage Divider

- LCD Drive Waveform – 1 Line Display (1/8 Duty Cycle)

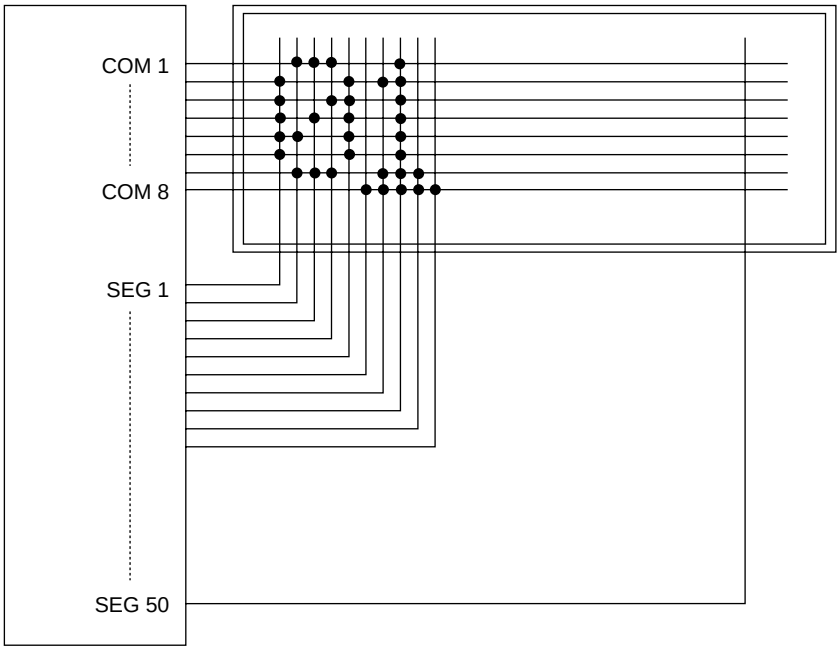


- LCD Drive Waveform – 2 Line Display (1/16 Duty Cycle)

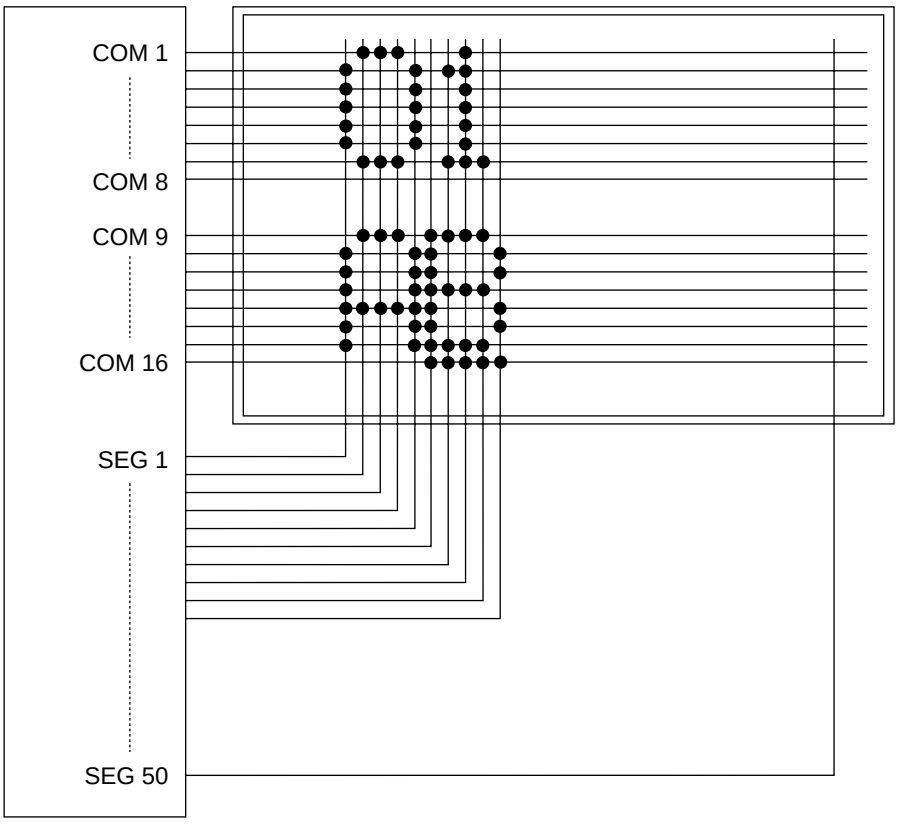


LCD Display Interface

- 10 Characters on 1 line (1/8 duty)

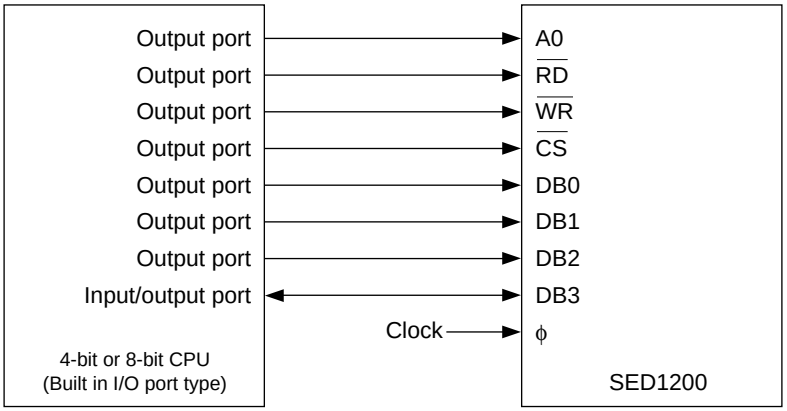


- 10 Characters on 2 lines (1/16 duty)

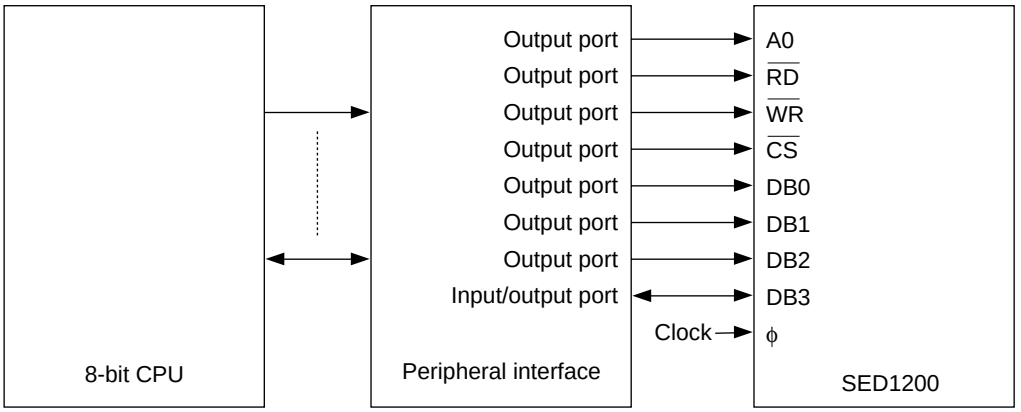


CPU Interface

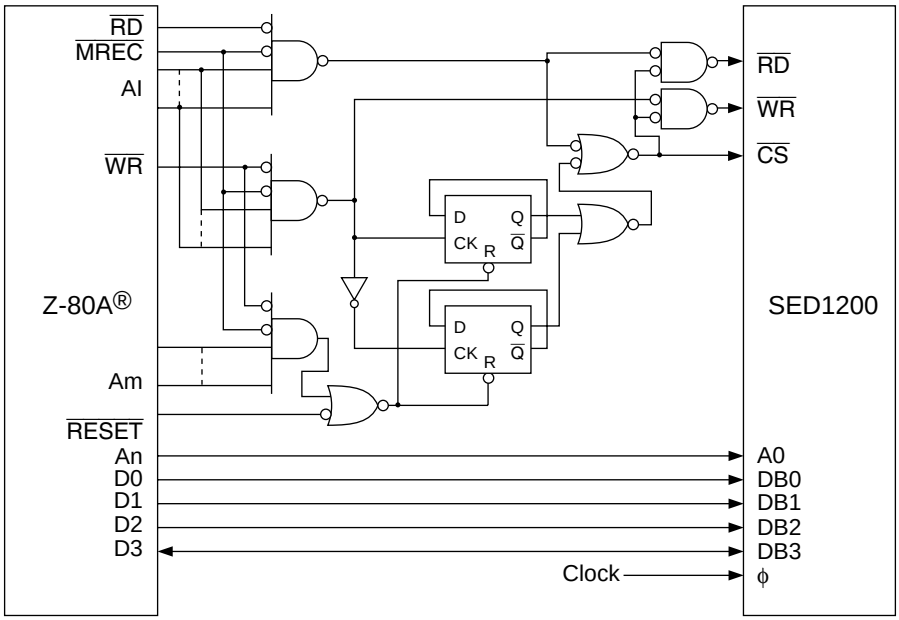
- 4-bits CPU with internal I/O port



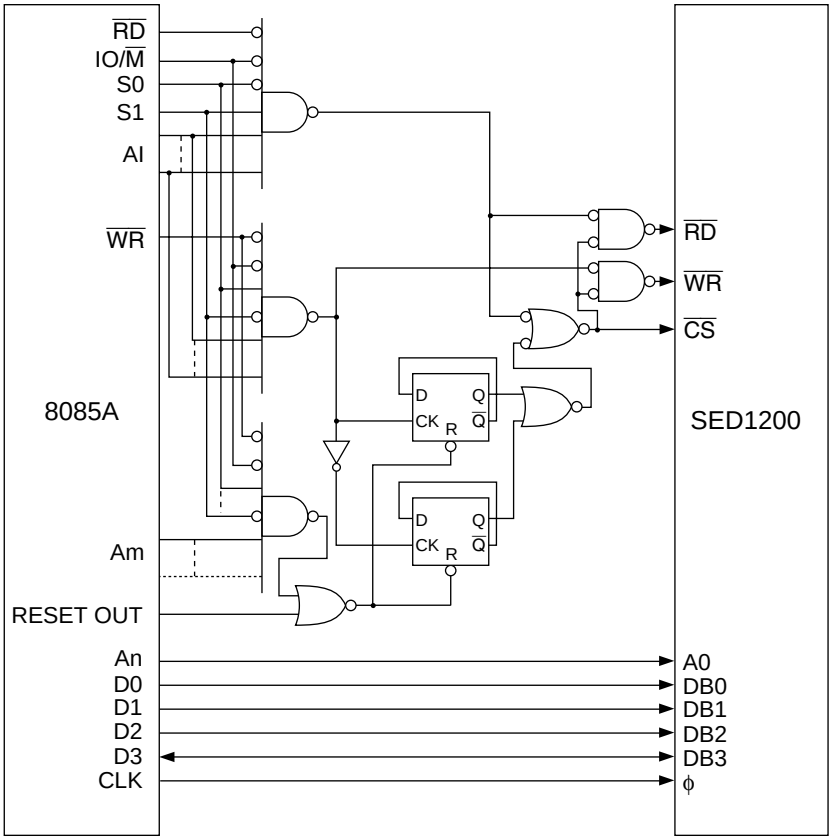
- 8-bit CPU with external I/O port



- Interface with Z-80A type CPU

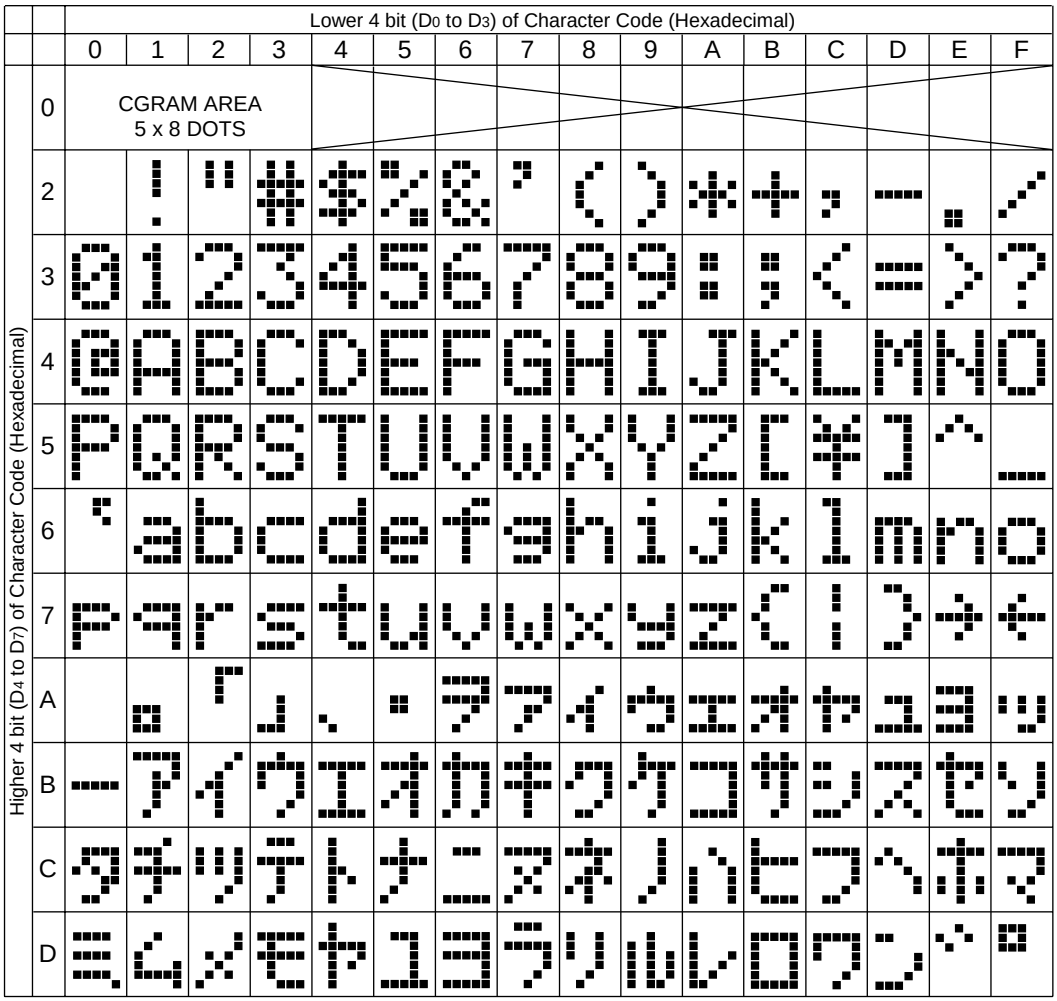


• Interface with 8085A type CPU

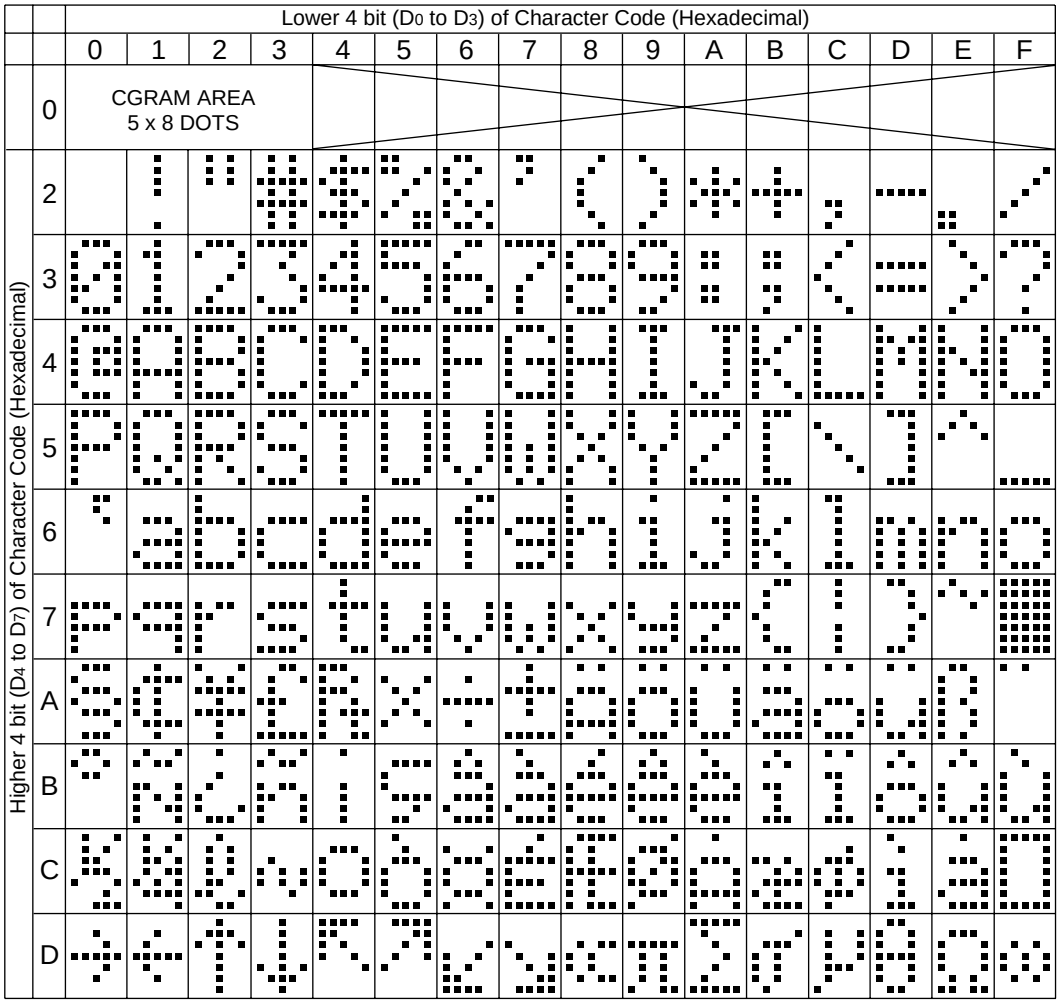


APPENDIX A: CHARACTER CODES AND FONTS

SED1200F0A/SED1200D0A

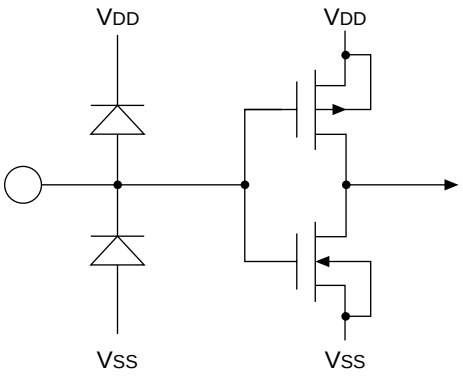


SED1200F0B/SED1200D0B

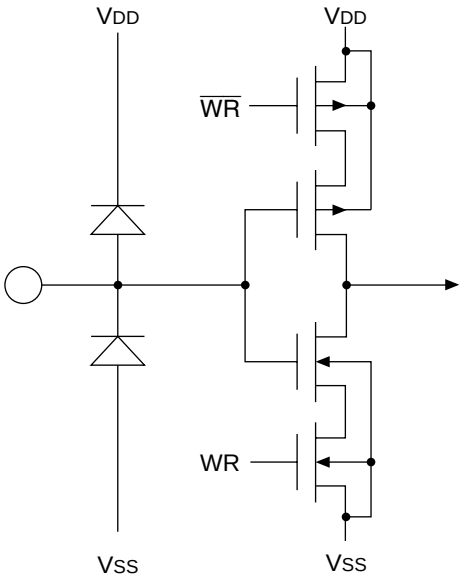


APPENDIX B: I/O TERMINAL STRUCTURE

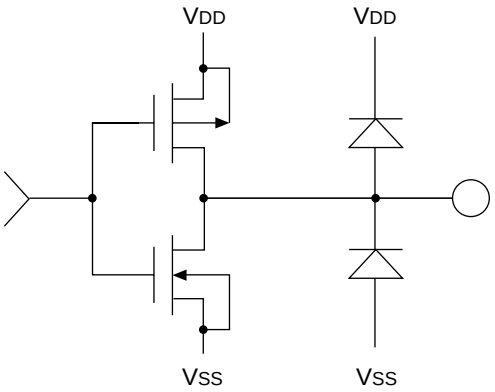
- Input Terminal (No pull-up)
  Terminals used: Φ, OSC1



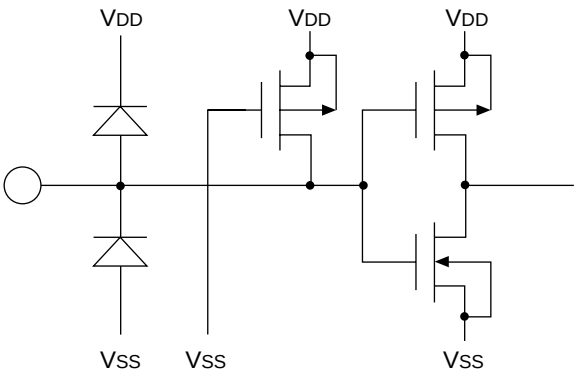
- Input Terminal (No pull-up)
  Terminals used: D0 to D2



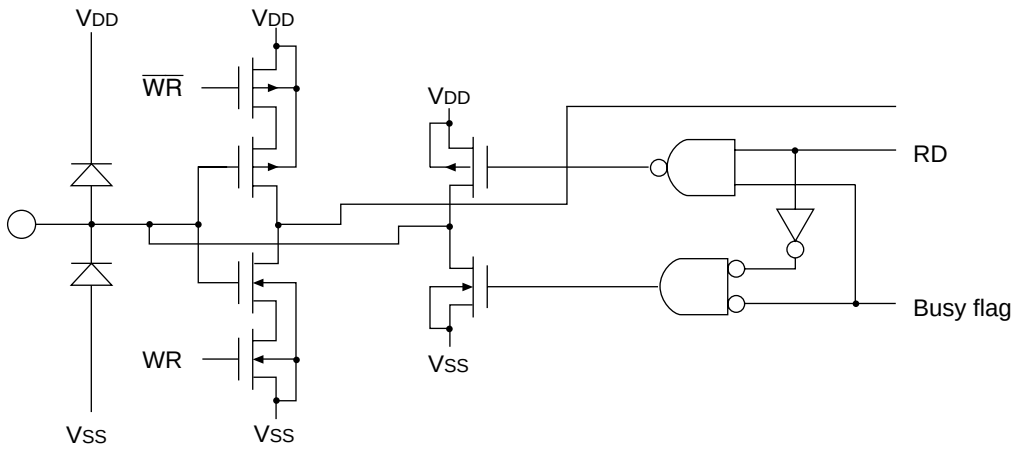
- Output Terminal (No pull-up)
  Terminals used: OSC2



- Input Terminal (Pull-up)
  Terminals used: $\overline{CS}$, $\overline{RD}$, $\overline{WR}$, A0



- I/O Terminal (No pull-up)
  Terminals used: D3



- LCD Drive Terminal (No pull-up)
  Terminals used: SEG1 to SEG50, COM1 to COM16